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A Proposal of a Forming-Free Resistive Switching Memory based on Breakdown and Anodic Reoxidization of thin SiO_2 on $NiSi_2$ Electrode using CeO_x Buffer Layer

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Abstract

A novel forming-free resistive memory with a large ON/OFF ratio of 10^4 is proposed based on breakdown and anodically reoxidized thin SiO_2 layer using CeO_x buffer layer and silicide electrodes. Low resistive state (LRS) is achieved by hard breakdown of the thin-SiO_2 layer owing to high dielectric constant of the CeO_x layer. By applying opposite bias to the electrode, high resistive state (HRS) can be reverted back by local anodic oxidation of the breakdown spot by high oxygen ion conductivity of CeO_x layer.

1. Introduction

Resistive memory has been focused as one of the non-volatile memories for next-generation, owing to low voltage and fast operation with excellent retention properties [1]. Base on the conductive-filament switching model, HRS and LRS are determined by the annihilation and creation of the oxygen vacancies at the tip of filaments within the oxides, which is commonly created during initial forming process [2]. The HRS/LRS ratio is strongly dependent on the forming process, and is sensitive to the compliance current as it determines the size of the filaments [3]. Forming-free devices have been presented using defect-rich AlON at the cost of HRS/LRS ratio [4]. We propose a novel structure to achieve forming-free, high HRS/LRS ratio and fast operation using a laminated structure of a thin SiO_2 with CeO_x buffer layer and silicide electrode.

2. Device Fabrication

Fig. 1 shows the structure of fabricated resistive switching devices, which consists of W top layer and CeO_x buffer layer. $NiSi_2$ was selected as a bottom electrode (BE) as pure-SiO_2 can be easily created and out-diffusion of Ni atom is suppressed [5]. For comparison, devices with TiN BEs were also fabricated as references. CeO_x films with different thicknesses were deposited on BEs by e-beam evaporation. Patterned W top electrodes (TE) with an area of $10\times10\mu m^2$ were used to measure the switching behaviors, including cycling tests and switching speed measurements.

3. Results and Discussion

Fig. 2 shows the current-voltage (IV) curve of devices with $NiSi_2$ BE. Initial forward and backward voltage sweep to positive voltage showed a change in resistive states from HRS to LRS. A sudden decrease in current with voltage application to reverse bias indicates a bipolar-type switching. By applying third voltage sweep to positive direction showed current behavior identical to the initial current, therefore a forming-free resistive switching is achieved. TEM image indicates the formation of 1.5-nm-thick SiO_2 between CeO_x and $NiSi_2$ BE, reactively formed by the catalytic effect of CeO_x [6]. On the other hand, devices with TiN BE required forming process for resistive switching, due to the formation of TiO_2, which has a high dielectric constant (fig.6). Therefore, silicide-BE to form a thin SiO_2 layer is the key to achieve forming-free operation. A model to explain the obtained switching behavior is shown in fig. 4. For set-process, high electric field induces a breakdown to the thin SiO_2, due to low dielectric constant (k~4), to change the state to LRS. For reset-process, oxygen ions from CeO_2 layer induce local anodic oxidation of the breakdown spot to create SiO_2 and change the state to HRS. The voltage to induce breakdown in the thin SiO_2 layer (V_{set}) can be explained by electrostatics with eq. (1~3), using hard breakdown field of SiO_2 (E_{BD}). Fig. 5 shows the IV curves of devices with different CeO_x thicknesses, and the V_{set} is summarized in fig. 6. Cyclic test and pulse switching measurement showed no degradation at least down to 200 nsec (limited to our measurement setup) with on-off ratio of 10^4, indicating the breakdown and oxidation can be reliably processed in a short period (fig. 7, 8).

Based on the above model, the requirements for material selection are discussed (fig. 9). For set-process, buffer high-k layer should have high dielectric constants to induce breakdown in thin SiO_2 layer, and high breakdown field so as not to form conduction filaments in the buffer high-k layer. Resistance of HRS is determined by the insulating property of SiO_2, so that silicides which form pure SiO_2 are preferable. For reset-process, buffer layer should have a high oxygen ion conductivity to induce anodic oxidation to the breakdown spots. As LRS is mainly limited by the electron conduction of buffer high-k layer, narrow bandgap is preferable to lower the resistance, which is usually the case for high-k materials.

3. Conclusions

We have successfully demonstrated a forming-free resistive switching behavior using a device with thin SiO_2 and a CeO_x on $NiSi_2$ electrode. Set and reset processes are achieved by breakdown of thin SiO_2 and anodic oxidation of the breakdown spot, so that it gives a high HRS/LRS ratio owing to the excellent insulating property of SiO_2.

References

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[4] W. Kim, et al., VLSI symp. tech., p. 22
[5] W. J. Strydom, et al., Solid-State Electron., 30, p. 947 (1987).
[6] T. Chikyow, et al., APL, 65, p. 1030 (1994).

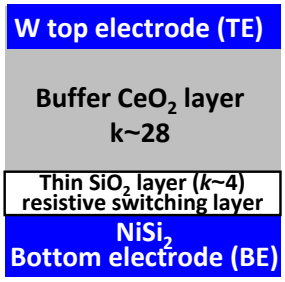

Fig.1 A schematic illustration of the fabricated resistive switching device. A thin SiO_2 layer is formed by oxidation of $NiSi_2$ BE.

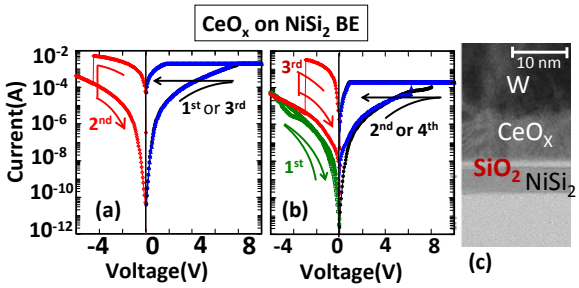

Fig.2 (a) I-V curve of the device with $NiSi_2$ BE shows a bipolar forming-free switching behavior; positive bias for set and negative one for reset. (b) No difference was observed under reverse initial voltage sweep. (c) Formation of a 1.5-nm-thick SiO_2 layer on $NiSi_2$ BE was confirmed by TEM image.

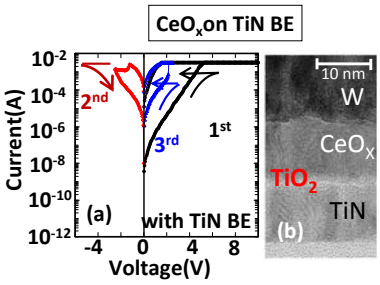

Fig. 3 (a) I-V curve of the device with TiN BE indicates the need of forming processes for resistive switching. TEM image reveals a formation of TiO_2 layer, which has high dielectric constant.

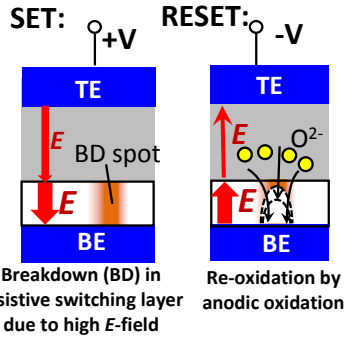

Fig.4 Owing to buffer CeO_x layer, high electric field induces breakdown to the thin SiO_2 layer during set process (+V). The layer also prompt the anodic reoxidation by oxygen ion diffusion to the breakdown spot with reverse voltage application (-V) from CeO_x layer. The resistance of HRS is determined by the excellent insulating properties of SiO_2.

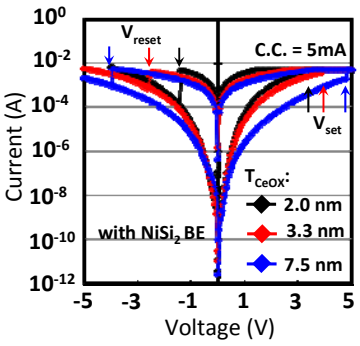

Fig.5 CeO_x thickness dependent switching behaviors with $NiSi_2$ BE. Smaller V_{set} and V_{reset} value were observed with thinner CeO_x thickness.

$$k_{SiO_2} E_{SiO_2} = k_{CeO_x} E_{CeO_x} \quad (1)$$

$$V_{app} = E_{SiO_2} t_{SiO_2} + E_{CeO_x} t_{CeO_x} \quad (2)$$

$$V_{set} = E_{SiO_2}^{BD} \left(t_{SiO_2} + \frac{k_{SiO_2}}{k_{CeO_x}} t_{CeO_x} \right) \quad (3)$$

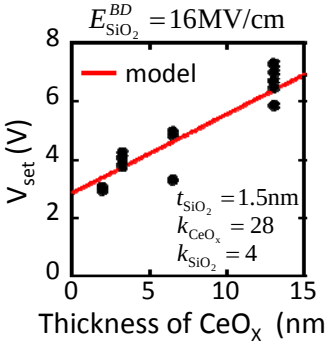

Fig.6 The CeO_x thickness dependency of V_{set} can be well explained by the electrostatics to induce hard breakdown field to thin SiO_2.

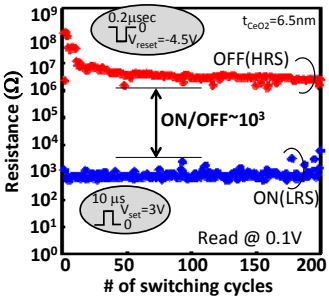

Fig.7 Cyclic switching endurance shows a stable HRS/LRS ratio of 10^3 with small spread for both HRS and LRS.

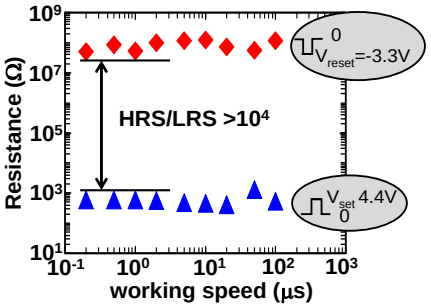

Fig.8 Resistive switching rate with different pulse width confirms no degradation in HRS/LRS at least down to 200nsec.

buffer layer: Example: CeO_x, TiO_2, YSZ, STO

- High *k* value
- High E_{BD} → induce BD in switching layer
- High oxygen ion conductivity → Easy for Re-oxidation process
- Small E_g → large current after breakdown of switching layer

Switching layer: Example: SiO_2 on Silicide BE

- Low *k* value
- Wide E_g
- Can be formed by anodic oxidation at BE

Fig.9. Summary of material equirements for buffer high-k, switching layers. Several possible candidates are also listed as examples.