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A Source-Side Injection Single-Poly Split-Gate Cell Technology for Embedded Flash Memory

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Abstract

An embedded flash memory using a source-side injection single-poly split-gate (SP-SPG) structure is proposed for the first time. A simple structure of SP-SPG is realized by using nanolithography technology to isolate gate electrodes, which results in remarkable reduction of the additional process cost. High performance and good reliability are also obtained with the isolation-gap size of 55 nm for a single cell.

1. Introduction

The embedded nonvolatile memory market is growing steadily with increase of micro-controller unit market for industrial, automotive and consumer applications. The source-side injection split-gate flash memory cell is one of the mainstream embedded flash technologies due to advantages of high efficient programming as well as low voltage read and no-over-erase structure. However, the conventional double-poly and triple-poly split-gate cells require significant modification to the standard logic process due to the complicated structure with a narrow isolation-gap between gate electrodes. In this paper, we present the single-poly split-gate cell technology to simplify the cell structure.

2. Cell Structure

Fig. 1 shows the equivalent circuit of a source-side injection (SSI) single-poly split-gate (SP-SPG) cell and schematic cross-sectional views of the SP-SPG and the conventional double-poly split-gate (DP-SPG) cells. The erase operation is achieved by FN electron tunneling. The split-gate cell consists of a floating-gate (FG) transistor and an access-gate (AG) transistor, which are arranged in serial between the drain (D) and the source (S) (Fig. 1 (a)). The FG is capacitively coupled to the N- well control-gate (CG) through the gate capacitor (C_g) (Fig. 1 (b)). The narrow isolation-gap is realized by using nanolithography technology. The drain diffusion profile is optimized for an erase operation. The DP-SPG structure produces the polysilicon encroachment in the gap region (Fig. 1 (c)) that reduces the hot electron injection efficiency and degrades the reliability.[1,2] In addition, the parasitic capacitance (C_p) between the AG and the FG causes the decrease in the gate coupling ratio. The SP-SPG structure makes it possible to shrink the isolation-gap without suffering from these issues. Long channel length of 0.3μm is used for both the AG and the FG transistors to evaluate the effect of isolation-gap width on cell characteristics.

3. Cell Characteristics

The high program efficiency can be obtained by a large lateral electric field (Fig. 1 (c)) across the channel in the gap region that is generated by controlling the AG transistor in the weak inversion region as shown in Fig. 2 and Table 1. The influence of isolation-gap width (S_{gg}) on the program efficiency (I_{inj}/I_d) and the cell threshold voltage (V_{th}) is evaluated using the grabber cell with the FG connected to the CG as shown in Figs. 3 and 4. Here, I_{inj} is the injection current into FG, and V_{th} is defined as the V_{cg} when the drain current is 10 μA. The program efficiency increases exponentially with decrease of S_{gg}. The grabber cell shows large increase in V_{th} with S_{gg} = 135 nm for the V_{ag} less than 5 V, which is improved by S_{gg} scaling-down less than 95 nm due to reduction of the resistance in the gap region. These results suggest the SP-SPG cell has the potential to satisfy high performance and good reliability due to its good scalability of the isolation-gap width. The program efficiency of the SP-SPG cell with the S_{gg} of 95 nm is larger by about 4 orders of magnitude as compared to the standard channel hot electron injection (CHEI) as shown in Fig. 5. The program speed is enhanced with increase of the drain voltage (V_d) and the programmed V_{th} is saturated in less than 1 μs with a low V_d of 4 V as shown in Fig. 6.

The program/erase endurance of 10^4 cycles is demonstrated for a single cell with the different S_{gg} as shown in Fig. 7. Little V_{th} window narrowing is observed without influence of S_{gg} for a single cell. Program disturb characteristics were also evaluated after 10^4 program/erase cycles for a single cell with a small S_{gg} of 55 nm. Even after stress time of 10 s, no V_{th} shift is observed for both the gate (V_{cg} = 16 V) and the drain (V_d = 5 V) bias-stresses (Fig. 8). These characteristics are acceptable for moderate-density embedded nonvolatile memory applications.

4. Conclusions

The SP-SPG cell with a good scalability of isolation-gap is fabricated without any special process, which will be lead to a wide range of embedded nonvolatile memory applications due to its low additional process cost as well as high performance and good reliability.

References

[1] S. Bhattacharya., IEDM Tech. Dig. (1996) 339.
[2] D. Shum et al., IMW (2012) 1.

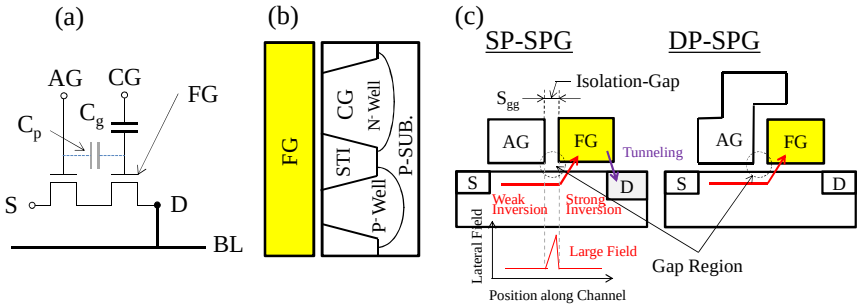


Fig.1. (a) Equivalent circuit of SP-SPG cell. (b) Cross-sectional view of SP-SPG cell along the control-gate-line (CG). (c) Cross-sectional view of SP-SPG and DP-SPG along the bit-line (BL).

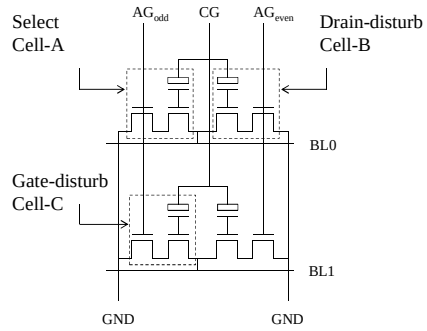


Fig. 2. Equivalent circuit of memory array.

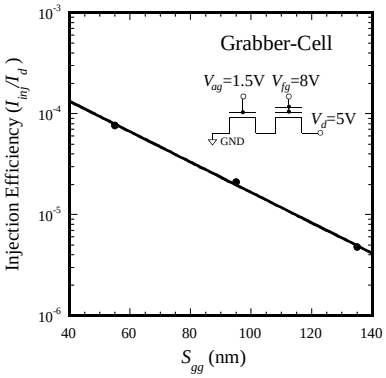


Fig. 3. Isolation gap size (S_{gg}) effect on Injection efficiency (I_{inj}/I_d). I_{inj} and I_d are the injection currents into FG and the drain current, respectively.

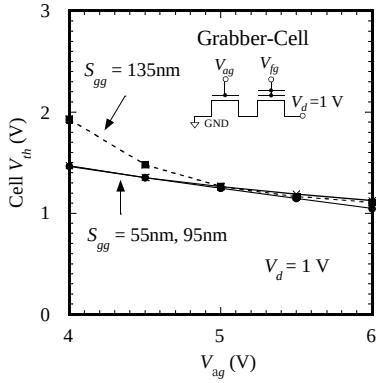


Fig. 4. Access gate voltage (V_{ag}) effect on cell V_{th}.

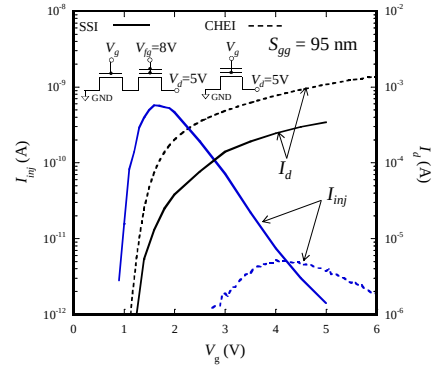


Fig. 5. Comparison of injection current (I_{inj}) into the FG and the drain current (I_d) between source-side injection (SSI) and channel hot electron injection (CHEI) programming.

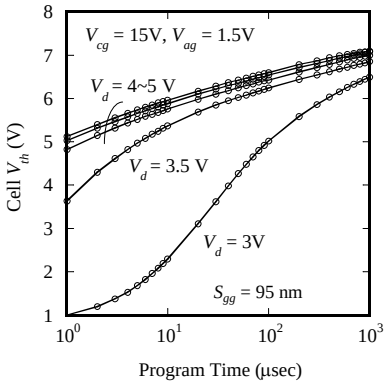


Fig. 6. Program time dependence of cell V_{th} for different drain voltage (V_d).

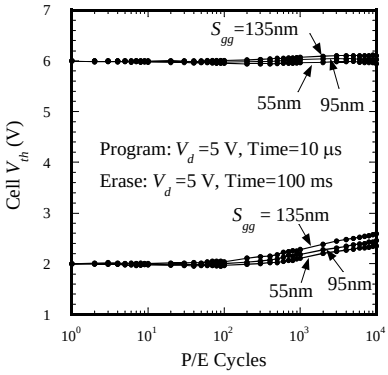
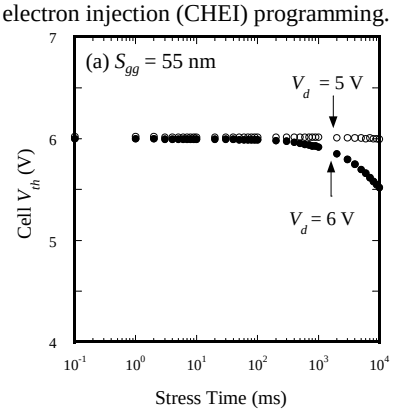


Fig. 7. Effect of program/erase cycle number on cell V_{th} for different isolation gap width (S_{gg}).



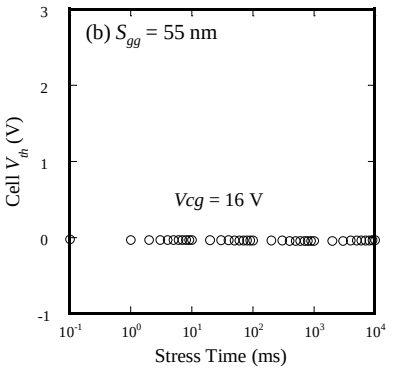


Fig. 8. Post-cycling program disturb characteristics for (a) drain and (b) gate bias-stresses.

Table. I. Typical operating conditions for the selected cell-A in the memory array shown in Fig. 2.

	AG_{odd}	AG_{even}	BL0	BL1	CG
PROGRAM	1.5 V	0	Vcc= 5 V	0	15 V
ERASE	0	0	10V	10V	0
READ	Vcc	0	1.5 V	0	Vcc