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Effect with Nano Dot Type Storage Layer Structure on Channel Region in 20nm Planar NAND Flash Memory Cell

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Abstract

The effect with changing from the floating gate type to the nano dot type storage layer structure on the cell current when they are programmed and erased state in 20nm Planar NAND flash memory cell is investigated. The nano dots concentrate the electric field from the control gate caused by the high electron density in a dot. Therefore, the fringing electric field when they are applied by positive gate bias from the source side to the channel region under the dot is decreased by about 18% at erased state. This leads to the decrease of the cell current at erased state by from 4 to 10μA. This indicates the importance of the design for the nano dots size and shapes in the storage layer.

1. Introduction

The nano dot type (ND) cell structures [1][2] cause discretely their threshold voltage shift by charging and discharging their nanoscale size (about 10nm or below) floating gate, because the threshold voltage shift is determined by electron tunneling and stored with quantum size effects, such as Coulomb blockade effect. Therefore, it is expected that those properties are applicable to be stable multi-level cell operation of NAND flash memory due to its separated threshold voltage's level fundamentally based on the quantum size effects. Although the floating gate type (FG) cell structure is widely used for a NAND flash memory, it is extremely difficult to be scaling its floating gate size down to about 10nm or below from the view point of their integration with high density as the NAND flash memory. Although the ND cells have been intensively studied, the investigation of the ND cell's performances for the NAND flash memory is not sufficient, especially focusing on their physical mechanisms caused by the storage layer structure. This paper presents the basic insight of the effect with the ND storage layer structure on the cell current with the programmed and erased state, and shows the importance of the inversion layer potential design by the size and shape of the nano-dot in the storage layer.

2. Simulated Structures and Method

Figure 1 shows the simulated device structures, (a) Floating gate type (FG), Nano dot type with (b) two dots, (c) three dots, and (d) four dots along the channel. Table I shows the device parameters setting. In this study, the dot space (Dsp) is 4nm in the ND cells ((b), (c), and (d)). The simulation is based on Sentaurus device simulator [3], and the drift diffusion model is used with nonlocal tunneling model based on [4] for program and erase operation.

3. Results and Discussions

Figure 2 shows the programmed threshold voltage (Vth) with respect to the program voltage (Vpgm) of the (a) FG and the ND cells ((b), (c), and (d)). These cells are programmed by applied the Vpgm of 10μsec pulse width with 1μsec rise and fall time. The Vpgm from the Vth from -1.0 to 1.0V is increased with changing storage layer structure from the (a) FG to the (d) ND about 0.9V. Figure 3 shows the erased threshold voltage characteristics with respect to the erase voltage (Verase) of the FG and the ND cells. Similarly, these cells are erased by applied the Verase of 10μsec pulse width with 1μsec rise and fall time. The Verase from the Vth from -1.0 to 1.0V is decreased with changing storage layer structure from the (a) FG to the (d) ND about 0.4V. Therefore, the ND storage layer structure is easy to erase rather than to program in this design. Figure 4 shows the threshold voltage shift with respect to the total stored charge in a cell. In Fig. 4, the total amount of the number of the electrons in a cell is the same between the FG and the ND cells. Therefore, the electron density in a dot is higher than that of the FG, moreover, the electron density in a dot is higher with the increase of the nano-dots in a cell. From these results, the number of electrons in the FG and the ND cells can be estimated by about (a) 624 per gate, (b) 5 per dot, (c) 2.5 per dot, and (d) 1.9 per dot in the case that the stored charge in the FG equals $1x10^{16}$ [C] as an example. Table II shows the evaluations of the NAND flash memory cell characteristics of the FG and the ND cells. The erased state and programmed state cell current are decreased by 10μA and 4μA, respectively, with changing the storage layer from the (a) FG to the (d) ND. The decrease of the cell current is caused by the decrease of the fringing electric field from the source side to the channel region under the dot due to its storage layer structure and high electron density in a dot. This results in the decrease of the electron density in the inversion layer by about 36% in Fig. 6. The electric field, potential, and electron density distributions after the programmed state in Fig. 7. In Fig. 7, the nano dots concentrate the electric field from the control gate, and affect the channel region under the dots. This indicates the importance of the storage layer design focusing on considering the nano dot's electric filed concentration. The possible electron injection mechanism is shown in Fig. 8. The potential field of the inversion layer has dip below the Si nano-dot, caused by the difference of dielectric constant between Si-nano-dot and SiO_2 dielectric layer under the positive gate bias. Then, this non-uniform potential profile induces the higher electron density area under the dot in inversion layer. It would assist the electron injection to the

dots. This means that the potential profile of electron inversion layer plays crucial role for the program operation of the ND cell. This mechanism tells us the important design parameters of the ND cells are the shape and the size of nano-dots, and the thickness of dielectric, because these parameters affect to the inversion layer potential under the gate bias.

4. Conclusions

As increase of the dots, the fringing electric field the source side to the channel region under the dots is decreased by 18%. This indicates the design insight for the ND cells as using the electric field concentration of dots with high electron density in a dot despite the same total amount of the number of electrons in a FG cell.

Acknowledgements

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References

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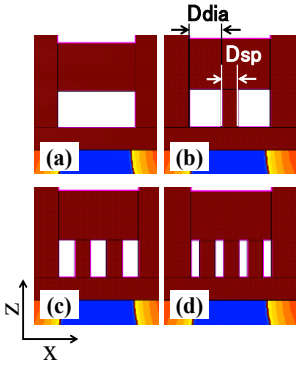

Fig. 1 Simulated device structures, (a) Floating gate type (FG), Nano dot type with (b) two dots, (c) three dots, and (d) four dots.

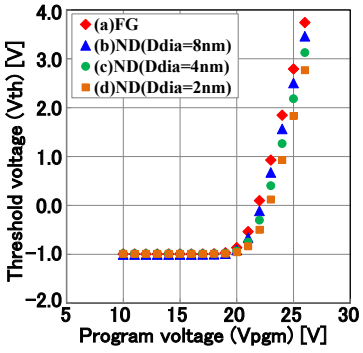

Fig. 2 Programmed threshold voltage characteristics of the FG and ND cells.

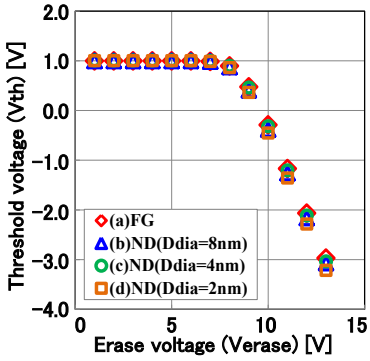

Fig. 3 Erased threshold voltage characteristics of the FG and ND cells.

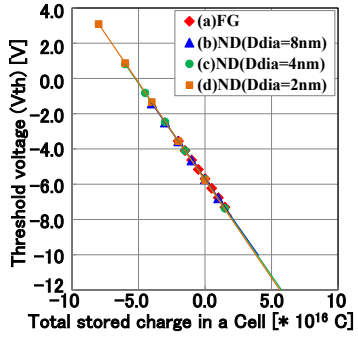

Fig. 4 Threshold voltage shifts with respect to the stored charge in a cell.

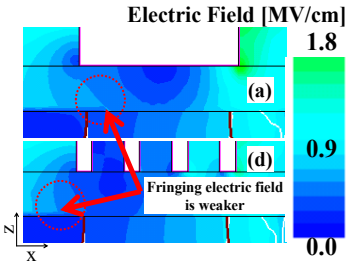

Fig. 5 Electric field distribution at erased state (Vth= -1.0V, Vgate= 5.0V).

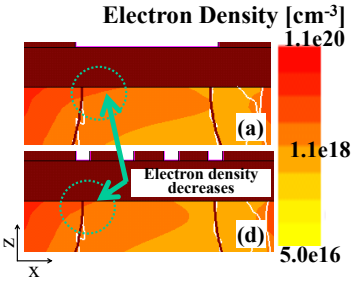

Fig. 6 Electron density distribution at erased state (Vth= -1.0V, Vgate= 5.0V).

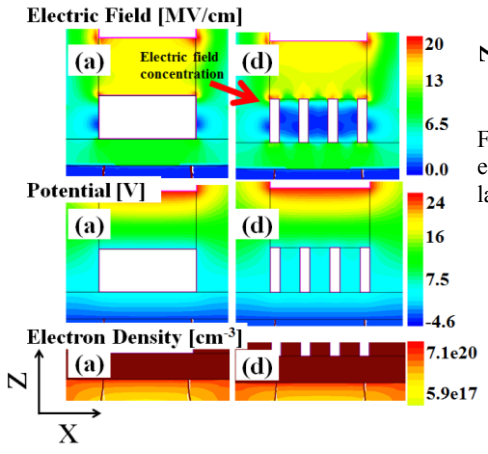

Fig. 7 Electric field, potential, and electron density distribution after applied by 10μsec Vpgm pulse width.

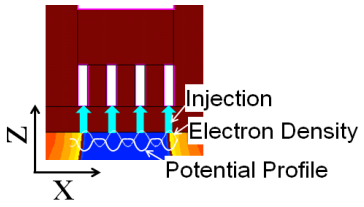

Fig. 8 Schematic of mechanism of electron injection from the inversion layer.

Table I. Device parameters setting

Device parameters	FG	ND
Gate length (Lg) [nm]	20	
Floating gate or Nano dot thickness (Tfg) [nm]	9	
Bottom oxide thickness (Toxb) [nm]	5.5	
Top oxide thickness (Toxt) [nm]	12	
Dot space (Dsp) [nm]		4
Dot diameter (Ddia) [nm]		2, 4, 8
Halo concentration (Nhalo) [cm⁻³]	1.5e18	
Channel concentration (Nch) [cm⁻³]	5e17	
Diffusion layer concentration (Nsd) [cm⁻³]	1e20	
Extension concentration (Next) [cm⁻³]	1e19	

Table II. Evaluation of memory cell characteristics

Evaluations	(a)FG	(b)ND (Ddia=8nm)	(c)ND (Ddia=4nm)	(d)ND (Ddia=2nm)
Erased state cell current [μA] at Vth =-1.0V, Vgate=5.0V	114	110	107	104
Programmed state cell current [μA] at Vth = +1.0V, Vgate=5.0V	35.3	33.3	32.1	31.0
Program voltage from Vth = −1.0 to +1.0 [V]	23.0	23.2	23.5	23.9
Erase voltage from Vth = +1.0 to −1.0 [V]	10.7	10.6	10.6	10.3