Extraction of Trapped Charge Profile in Space and Energy in P-Channel SONOS Memory Device

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Abstract. In this work, we demonstrate a trapped charge decay model based on trap-to-band (T-B) tunneling and thermal excitation (TE) detrapping mechanisms. The trapped charge profile in space and energy is successfully extracted, for the first time, by analyzing the charge loss phenomena under gate stress from $V_G = -5$ to 5 V at room temperature. Subsequently, the extracted charge profile is also applied to analyze the retention characteristic up to $\sim 10^7$ s at 150° C, which shows good agreement with measured data. It can be concluded that the trap energy is below ~ 1 eV from conduction band, and the trapped charge centroid is located at the center of SiN along the vertical direction.

1. Introduction

Many studies have been done for trap profiling techniques during Fowler-Nordheim (FN) program in n-channel SONOS device [1,2]. Some of them monitored long-term data retention that can be used to extract the charge profile [3]; others directly probed the traps by low-frequency charge pumping [4]. However, the space and energy distribution of the trapped charges induced by channel hot hole induced hot electron injection (CHHIHE) in p-channel SONOS has not been explored extensively. Previously, we proposed a transient analysis method to examine the spatial charge profile in SiN along the channel direction [5]. In this work, the space and energy profile along the vertical direction is further investigated.

2. Device Structure, Bias setting, and Methodology

The program operation of p-channel SONOS is presented in Fig. 1. Electron-hole pairs are generated by impact ionization, and subsequently electrons uniformly distribute in SiN after surmounting bottom oxide (BO), as shown in Fig. 1(a) and 1(b)[6]. Figure 1(c) shows the I-V curves of the measured p-channel SONOS device after programming. The forward and reverse read show the same curve, which means electrons uniformly distribute in SiN layer [5]. As a consequence, the lateral localization effect can be neglected, which allows us to mainly focus on the vertical charge re-distribution during gate stress and baking.

In our numerical calculation, the trapped charge profile is partitioned into many sub-regions in space and energy, as shown in Fig. 2. Two major detrapping mechanisms occur in SONOS device, one is T-B tunneling through either BO or top oxide (TO), and another is via thermal emission and subsequent oxide tunneling. Equations for calculating the charge decay mechanism are shown in Table I. The trapped charge can be expressed as:

$$n_t(\phi_t, t) = n_t(\phi_t, 0) \cdot e^{-t/\tau}$$
(1)

where ϕ_t is the trap level, $n_t(\phi_t, 0)$ is the initial trapped charge density after programming, and τ is the detrapping time constant. The time constant is calculated as the sum of the contributions due to tunneling through bottom oxide $\tau_{T-B}(x, \phi_t)$, top oxide $\tau_{T-B}'(x, \phi_t)$, and oxide tunneling by thermal emission $\tau_{TE}(x, \phi_t, T)$:

$$\frac{1}{\tau} = \frac{1}{\tau_{\tau-B}(x,\phi_t)} + \frac{1}{\tau_{\tau-B}'(x,\phi_t)} + \frac{1}{\tau_{\tau E}(x,\phi_t,T)}$$
(2)

where x is the coordinate along the vertical direction, T is the temperature [1, 3]. Flowchart for the calculation is shown in Fig. 3. Firstly, setup the initial charge profile after programming. Then,

calculating the charge loss during the time step Δt , and the resulting state at the end of each time step is used to solve again the Poisson equation. Subsequently, recalculating and updating the profile and the detrapping time constant. Finally, the ΔVt by charge loss is calculated and is compared with measured data. The parameters used in our model are given in Table II.

3. Simulation and Experimental Results

The spatial and energy distribution of the trapped charges after programming is extracted by analyzing the charge loss data under gate stress from $V_G = -5$ to 5 V, shown in Fig. 4(a). The trap energy is below ~1 eV from conduction band, and the trapped charge centroid is located at the center of SiN. Next, Fig. 4(b) shows the charge profile after 90 s gate stress under $V_G = -5$ V at room temperature. Third, Fig. 4(c) shows the profile after 10^5 s at 150° C baking. Under the condition of $V_G = -5$ V, the trapped charges are mainly tunneling through BO. This is because the charge decay is dominated by τ_{T-B} . In the case of retention characteristic, only the shallow trapped charges are prone to be thermally excited at 150° C. This observation can be attributed to the smaller τ_{TE} . Simulated results of gate stress and 150°C baking show good agreement with experimental data as shown in Fig. 4(d) and 4(e). Next, in order to examine other possibilities of trapped charge profiles, two cases with the charge centroid near the TO or BO are simulated, as shown in Fig. 5(a) and 5(b). The related simulated results are shown in Fig. 5(c) and 5(d). Both of them show inconsistent result between measurement and simulation. Similarly, even modifying energy distribution, it cannot fit the measurement result. Fig. 6(a) and 6(b) show the simulated evolution in time of the charge profile and band diagram in SiN along the vertical direction under $V_G = -5V$ gate stress. The total stress time is 90 s. Fig. 7(a) and 7(b) show the case of retention at 150 °C and the range is from the initial state to 10^7 s.

4. Conclusions

In this work, we proposed a comprehensive method to extract the spatial and energy distribution of the trapped charges, and obtained good agreement both with gate stress and high temperature baking. This method provides the thorough understanding of the detrapping modes for various bias and temperature conditions. It is generally applicable for all kinds of SONOS devices.

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Fig. 1. (a) Program operation of p-channel SONOS. (b) The injected charges quickly spread over the whole channel area uniformly after 7 steps of the ramping programming. (c) Comparison of the measured I-V curves in forward and reverse read in program state.



Fig. 2. Illustration of the discretization scheme in the trap energy and space for numerical simulation.



Fig. 3. Flowchart for the calculation.

Table I. Equations for calculating SiN charge trap and, time constants for trap to band tunneling and thermal emission.

Table II. Parameters used for the numerical simulation.





Fig. 4. (a) Spatial and energy distributions for trapped charges after programming. (b) The charge profile after 90s under V_G =-5V gate stress. (c) The charge profile after 10^5 s 150° C baking. (d) Simulated V_{th} shift by gate stress comparing with measurement data. (e) Simulated retention characteristics by 150° C baking comparing with measurement data.

Fig. 5. (a, b) Two arbitrary charge distribution after programming. (c, d) The related simulated gate stress and retention loss curves.



Fig. 6. Simulated evolution of (a) the spatial charge distribution and (b) the conduction band during $V_G = -5 V$ gate stress between initial state and 90 s.



Fig. 7. Simulated evolution of (a) the spatial charge distribution and (b) the conduction band during retention between initial state and 10^7 s.