An 8-ch, 20-V Output CMOS Switching Driver with 3.3-V Power Supply for Integrated MEMS Devices Controlling

Motohiro Takayasu¹, Atsushi Shirane¹, Sangyeop Lee¹, Daisuke Yamane¹, Hiroyuki Ito¹, Xiaoyu Mi², Hiroaki Inoue², Fumihiko Nakazawa², Satoshi Ueda², Noboru Ishihara¹ and Kazuya Masu¹

¹ Solutions Research Laboratory, Tokyo Institute of Technology 4259-S2-14 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan Phone: +81-45-924-5031 E-mail: paper@lsi.pi.titech.ac.jp

² Fujitsu Laboratories LTD, Association of Super-Advanced Electronics Technology

10-1 Morinosato-Wakamiya, Atsugi, Kanagawa 243-0197, Japan

Abstract

An 8-ch output switching driver has been implemented for integrated MEMS (Micro Electro Mechanical Systems) devices controlling by using the 0.18-µm CMOS process technology. The driver can output 20-V switching signals for 1-nF capacitive loads with 3.3-V power supply. To get high output voltage exceeding the transistor's breakdown voltage, optimal transistor-well-biasing techniques for triple-well-structured n-MOS transistors, employed in the charge pump and the discharge circuits, has been investigated.

1. Introduction

Diverse integration of MEMS and CMOS is attractive to implement miniaturized systems with high performance and high functionality. In the RF systems, use of MEMS devices, such as switches, varactors, inductors, actuators and so on, make it possible to realize low-loss wide-band tunable filters with small size [1, 2, and 3].

In this paper, an 8-ch output CMOS switching driver is proposed for integrated MEMS devices controlling. To control the active MEMS devices controlled by the electric field, high voltage signals more than 15-V are required usually. But they are difficult to be generated from the conventional circuit using the standard CMOS LSI process technology. The maximum output voltage is limited by the transistor's breakdown voltage. In the 0.18-µm CMOS process, break down voltage of pn junction between drain and back-gate (well) terminals is less than about 11-V. To overcome this problem, triple-well-structured n-MOS transistors are employed in charge pump and discharge circuits, and optimal biasing techniques, for p-well and deep n-well, are clarified, and thus the driver can output 20-V switching signal with 3.3-V power supply.

2. 8-ch output switching driver

A proposed 8-ch driver is shown in Fig.1. The driver is consisting of eight sets of charge pump and discharge circuits, an oscillator and a control logic circuit. The charge pump circuit steps up the voltage from the power supply voltage of 3.3-V to the output voltage of 20-V using differential clock signals from the oscillator. The discharge circuit pulls down the output voltage for capacitive loads, such as MEMS switches or varactors controlled by the

electric field.

The charge pomp circuit is shown in Fig.2 comparing with the conventional one [4]. In the conventional circuit, voltage between the output node (Mn drain) and back-gate terminal (p-well of Mn) connected to the ground become maximum. Therefore, the maximum output voltage is limited by the breakdown voltage of the pn junction as previously described in section 1. To get higher output voltage, following techniques are applied in the proposed circuit.

(i) Triple-well-structured n-MOS transistors are used for MOS diodes to bias each back-gate (p-well) independently. (ii) And p-well and deep n-well biases of each transistor, in the latter stages, are set to be high using previous charge pump stage's output voltage to enlarge the maximum output voltage, keeping the condition that each p-well-bias is smaller than each deep n-well bias [5].

(iii) Breakdown voltage of capacitor also limits the maximum output voltage. To prevent this, clock signals at latter charge pump stages use previous stage's output signals [4].

To get 20-V output, eleven charge pump stages are cascaded.

The discharge circuit is shown in Fig. 3. Cascaded transistor structure is used to reduce the voltage between the drain and source terminal of each transistor. And p-well and deep n-well biases of each transistor are set optimal considering breakdown voltage to enlarge the maximum output voltage, keeping each p-well-bias is smaller than each deep n-well bias.

In the oscillator, to get differential signals as clocks for the charge pumps, differential inverter type circuit is employed.

Fig. 4 is showing the simulation results showing the output switching characteristics. Simulation is done by using transistor model including the breakdown characteristics. The conventional circuit output voltage is limited by the breakdown voltage. But the proposed circuit can output about 20-V that is twice of the conventional one and is exceeding the breakdown voltages; 11-V between the drain and back-gate (p-well) terminals and 15-V between p-well and deep n-well.

3. Fabrication Results

To confirm the validity of the proposed circuit technique, the 8-ch output driver was designed and fabricated by using 0.18- μ m CMOS process technology. Circuit parameters, such as transistor sizes, capacitor values, oscillation frequencies, are optimized to be able to drive 1-nF capacitive load with rise and fall time less than 100- μ s. 44.8-pF MIM capacitors were used for each charge pump. Oscillation frequency was determined to be 110-MHz to satisfy the rise and fall time condition. A fabricated chip micrograph is shown in Fig.5. Core circuit area is 2290×3390- μ m².

Measured output wave form is shown in Fig. 6. 20-V switching signal was successfully obtained. Similar outputs were obtained at every 8-ch outputs. Each output signal can be controlled independently.

Measured results are summarized in table I.

4. Conclusions

To get high output voltage signal exceeding the transistor's breakdown voltage, optimal transistor-well-biasing techniques for triple-well-structured n-MOS transistors are demonstrated and the validity was confirmed by fabricating the 8-ch, 20-V output CMOS switching driver that can be operated with 3.3-V power supply.

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Fig. 5 Chip micrograph (2290×3390-µm²).



Fig. 6 Measured output wave form for 1.3-nF load.



< 2400×3500-µm²

0.18-um

2290×3390-µm²

0.18-µm

Chip size

CMOS process