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Novel Dynamic Reconfigurable FPGA based on Multi-Context Scheme Using One-Time Memory with Gate-Induced Permanent Path

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Abstract

We present a multi-context based dynamic reconfigurable FPGA (MC-DPGA) that is smaller than conventional FPGA. To mitigate the memory area, novel one-time programmable (OTP) memories based on standard CMOS transistors are employed to configuration memories. Since different terminals are used in programming and in reading unlike conventional OTP memories, it is simple to embed the configuration memories in logic circuits. We have estimated the mapping area using 10 benchmark circuits, and confirmed that the area of MC-DPGAs is reduced by 30 % on average.

1. Introduction

A field programmable gate array (FPGA) is an integrated circuit that can be programmed after manufacturing. Recently, FPGA is used in various applications since the development cost of application specific integrated circuit (ASIC) becomes too high. In order to use FPGA in place of ASIC, logic density is a major concern, especially in high-end FPGA. Although conventional FPGA uses most advanced CMOS process technology, it comes to be difficult to extend logic density sufficiently due to process complexity. Therefore, circuit technology to achieve higher logic density is expected.

MC-DPGAs are expected as a method of increasing the logic density [1]. Figure 1 shows the simplified schematics of conventional FPGAs and MC-DPGAs. The conventional FPGAs have only one configuration memory corresponding to a logic circuit. Therefore, once the memories are configured, the logics perform particular functions unless reconfigured. In contrast, the MC-DPGAs have multiple memories corresponding to a logic circuit, thereby logic circuits can perform different functions by switching the reading memories. Thus, MC-DPGAs reuse the hardware resource. The additional memories and control circuit, however, may cause the increase in area. In particular, conventional configuration memory in advanced CMOS process is SRAM, the area of configuration memories significantly influences the area of MC-DPGA. Although previous works have proposed an architecture level solution to reduce the overhead in MC-DPGAs [2], the method is not always effective since its efficiency depends on the circuit configured in FPGA.

In this work, we present the novel MC-DPGA using specific configuration memory. The memory that we propose in this paper is small, one-time programmable and three-terminal-device that makes easy to programming/reading operation. Furthermore, the memory can be fabricated by using standard CMOS process, thus it is suitable for high-end FPGA using advanced CMOS process. We have designed MC-DPGA circuits and developed a placement and routing tool to estimate the proposed MC-DPGA area, and clarified that the area of MC-DPGA can be reduced compared with conventional FPGA.

2. Memory device and circuit

Figure 2 shows the cross-sectional view and the explanation of the programming operation of the memory device. The memory is a transistor fabricated by standard CMOS processes technology. As shown in Fig. 2(a), when negative programming voltage is applied to the control gate, and ground voltage is applied to the source and drain, PN junctions between the channel region and source/drain are successfully broken. In this state, as shown in Fig. 2(b), source and drain of the memory transistor are shorted electrically. In addition, it is confirmed that the rectifying property due to the PN junction remains between the substrate and the drain. Therefore, additional leakage current can be avoided by using these memories during FPGA operation.

Figure 3 shows the multi-context memory circuits. The

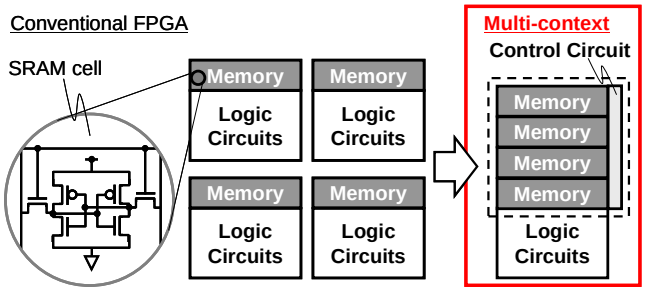

Fig. 1 Overview of conventional and MC-DPGA.

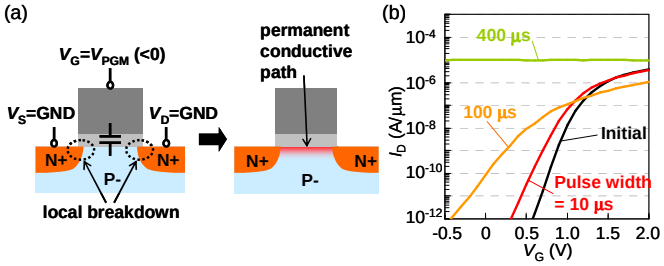

Fig. 2 (a) Cross-sectional of memory. (b) Change in drain current after the program voltage is applied.

configuration data of the memory is read by switching on one of the selection transistors. Our one-time configuration memory (OTCM) consists of two memory device pairs. One is programmed to shorted state while the other is kept in initial state. When using an OTCM, power supply voltage and ground voltage are applied between two devices, and ground voltage is applied to the gate of both devices. Configuration data output as a logic signal depends on the difference of the resistance between two devices.

Since SRAM is volatile, the read current may disturb the data of SRAM cells. Therefore, as shown in Fig. 3(a), SRAM based multi-context circuit requires read buffer in each SRAM cell, which results in significant area overhead with the number of context memories. On the other hand, our configuration memories are smaller in area than SRAM-based configuration memories since our memories are nonvolatile.

In MC-DPGA, reading cycle of configuration memory must be faster than user clock to avoid the degradation of FPGA performance. Figure 4 shows the result of SPICE simulations of read operation of our multi-context memory circuit, calculated with 22 nm Predictive Technology model [3,4]. The nominal power supply voltage is 0.8 V. Since we suppose nMOS pass transistor, 1.2 V boosted voltage is applied to the gate to pass logic high value. As shown in Fig. 4, the memory operation is feasible at a frequency as high as 1 GHz. Therefore, maximum user clock (250 MHz) is sufficient for high-end FPGA in comparison with conventional FPGA.

3. Area Estimation

We have built placement and routing (P&R) tools for MC-DPGAs to evaluate the area. Since the computation sequence of each logic circuit must be considered in multi-context dynamic reconfigurable logic, we have applied sequence constraint to conventional simulated annealing method to optimize the placement. The number of occupation transistors for each benchmark circuit is used for area comparison. Figure 5 shows the calculation results of placement with 10 benchmark circuits. The results for conventional FPGA are also shown in Fig. 5. It is confirmed that the area of MC-DPGA becomes smaller than conventional FPGA at the certain number of context by using our memories.

Figure 6 shows the area comparison of the average of the placement results with 10 benchmark circuits. As shown in Fig. 6, all MC-DPGAs with SRAM cells are larger in area than conventional FPGA. This is because SRAM cell is too large to use in multi-context memories. Therefore the area for multi-context memories becomes dominant in FPGA, and the benefit of multi-context scheme is vanished. In contrast, MC-DPGAs with our OTCMs are smaller in area than conventional FPGA because we have successfully designed configuration memory circuits using small OTCMs. The area is minimized at four contexts, which results in 30 % area reduction on average compared with conventional FPGA.

4. Conclusion

We have proposed the novel MC-DPGA using small configuration memories constructed by standard CMOS transistors. We have designed the circuits and built the P&R tools for MC-DPGA to estimate the area. The area of proposed MC-DPGAs is reduced by 30 % on average. Proposed MC-DPGA is an effective technology to enhance the logic density in future high integration FPGA.

References

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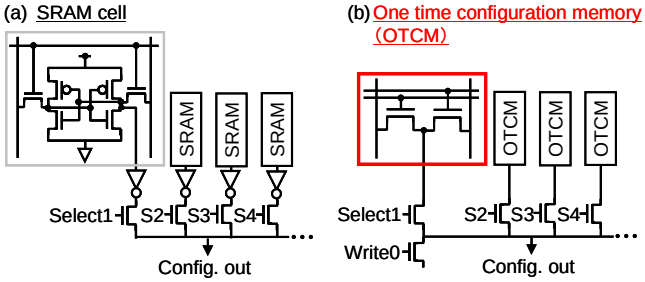

Fig. 3 Simple multi-context memory circuits with (a) SRAM cells and (b) OTCMs.

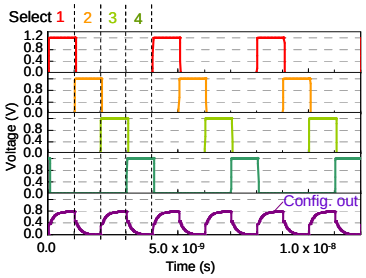

Fig. 4 SPICE simulations of the multi-context memory circuit shown in the Fig. 3(b).

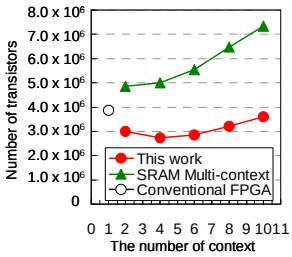

Fig. 6 Comparing the average of the results of placement with 10 benchmark circuits.

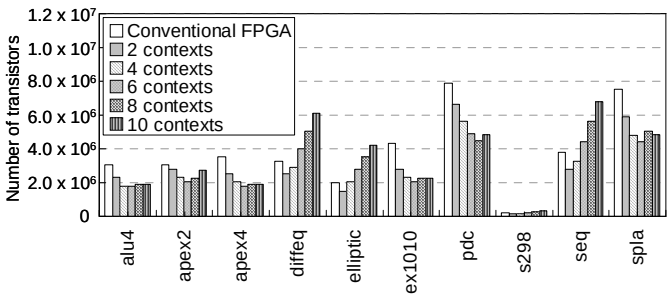

Fig. 5 Area estimation of MC-DPGA in 10 benchmark circuits.