

A High-Voltage Isolated Current Sense Amplifier for Fully CMOS Compatible Non-volatile Memories

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Abstract—A high-speed current sense amplifier (SA) blocking 8.3V during program/erase of the CMOS compatible non-volatile memories is proposed and fabricated using the standard 0.35 μ m CMOS process. After the memory cells are programmed, the measured access time is as fast as 13ns for the current difference of 3 μ A at $V_{DD} = 3.3V$.

1. Introduction

The recent trend of embedded non-volatile memories (NVM) includes resistive RAM (RRAM) [1], magnetoresistive RAM (MRAM) [2] and ferroelectric RAM (FeRAM) [3]. They can be integrated with the standard CMOS logic processes with shorter program/erase times than those of the conventional flash memories. However, the extra masking and processing steps may result in raised cost and degraded yield.

To have the cost-effective embedded NVM without the extra processing steps or design rule violation, this paper utilizes the multiple time programming (MTP) [4] cells using the standard TSMC 0.35 μ m CMOS process. The MTP Cell composed of two 3.3V NMOS transistors in series is shown in Fig. 1. The operation conditions are listed in Table I. Since the BL nodes could be biased at 8.3V or 0V, the SA connected to the BL nodes may be overstressed during program/erase owing to $V_{DD} = 3.3V$. Thus, the high-voltage (HV) isolation circuits are required to avoid damage of the SA.

2. System Architecture

Figure 2 illustrates the system architecture of the test chip to control a NOR type MTP memory array. “din” and “dout” are the input and output data. The WL, BL and SL drivers provide the corresponding biases for word lines (WL), bit lines (BL) and source lines (SL), respectively. The HV isolation circuit is placed between the BLs of memory array and the current SA to ensure the device reliability. This paper presents the design technique of the circuit blocks marked by the bold lines in Fig. 2.

3. The Sense Amplifier with High-Voltage Isolation

The proposed current SA sinks the current from the BL to Node blin as shown in Fig. 3, where the RL means the bit line of the reference cell which generates the reference current. Two HV isolation circuit blocks are inserted between the bit lines and the SA. The detailed circuits are sketched in Fig. 4(a) with the bias conditions listed in Table II. The symbols of NMOS or PMOS transistors with the thick lines at the gates represent 5V transistors. The two inputs T0 and reset determine the node voltages of iso1 and iso2. The output buffer controlled by T1 is a dynamic latch as shown in Fig. 4(b). The timing diagram of the SA

including the circuits in Fig. 4 is illustrated in Fig. 5.

The read operation is divided into three phases, *i.e.* reset, equalize, and sensing. In the reset state, sal, sar, blin and rlin in Fig. 3 are reset to 0. During equalize, the MTP and reference cell currents enter the SA, while sal and sar are equalized to about $V_{DD}/2$ due to saeq= V_{DD} . The small current difference makes blin and rlin slightly different. In the sensing phase, saeq turns off the switch between sal and sar, which are then amplified. After sar and sal have some difference, T1 becomes V_{DD} , and the output data is latched in the output buffer, which may need extra delay due to parasitic effects such as pads and package. After the data is latched at the output and before the next read begins, it is the idle state as shown in Fig. 5.

The HV isolation circuit can protect the SA from the high voltage stress of bit lines during program/erase, which corresponds to “isolation” in Table II. Because T0 and reset are 0V, the NMOS’s are off and PMOS’s are on as shown in Fig. 4(a). That results in $V_{DD}=3.3V$ transferred to iso1 and iso2. When the BL is 8.3V, the voltage drop between BL and iso1 and iso2 are 5 V, which is within the safe margin of the 5V MOS transistors. On the other hand, during read, the BL, blin and rlin are reset to 0 owing to T0 = reset = V_{DD} . Then, the “reset” signal becomes 0 to allow the cell current flows from the BL to the SA.

4. Simulation and Measurement Results

The simulated waveforms to read one of the memory cells after programming logic 1 are shown in Fig. 6, in which the control signals, saeq, reset, T1 are in the lower panel. Nodes sal, sar, and dout are close to 0V during reset. Then, sal and sar are equalized and pulled to nearly $V_{DD}/2$ at the equalize state. The sensing operation is started right after saeq=0, and the output buffer is activated by T1= V_{DD} when the difference between sar and sal is large enough.

The chip microphotograph of two SA’s with HV isolation marked by white lines is shown in Fig. 7. Fig. 8 demonstrates the measured waveforms of the output (dout) and the control signals (reset, Saeq, T1) for reading logic 1 from different cells consecutively and reset to 0V alternatively. According to the definitions in Fig. 5, the sensing operation includes 3ns of reset, 6ns of equalize, and 2ns of sensing. That means the access time (AT) is 11ns by simulation. However, it becomes 13ns by measurement because of the parasitic effects of package and measurement systems. The outputs need more time to reach the full swing. That is why the slow rising and falling waveforms of “dout” appear.

Table III lists the performance comparison of the recent published SA’s used in non-volatile memories. The sensing delay time (SDT) of the proposed SA with the HV

isolation circuit is 1.4ns at sensing current (SC) of 3 μ A with C_L of 0.5pF. Besides, the measured access time is shorter than that in Ref. [8].

5. Conclusions

This paper proposes a current SA with HV isolation circuit design techniques to avoid high voltage stress for the CMOS compatible memories using TSMC 0.35 μ m CMOS technology. Both the memory cells and the circuits were designed without violating the design rules. Owing to equalizing of the SA to $V_{DD}/2$ to enhance the sensing speed, the simulation and measurement results of the test chip show the SDT=1.4ns and AT=13ns when SC=3 μ A. We can expect it can be applied to almost all types of embedded memories without reliability issues.

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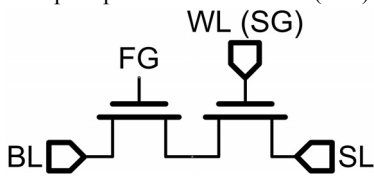


Fig. 1 Schematic of a MTP cell

Table I Bias conditions of the MTP cell

	BL (V)	WL (V)		SL (V)	Time
		select	un-select		
Prog.	8.3	4	0	0	10ms
Erase	8.3	1	0	0	10ms
Read	0~0.5	1.8	0	1.8	<15ns

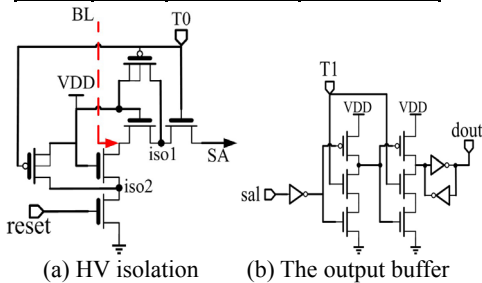


Fig. 4 The 2 circuit blocks in Fig. 3

Table II Bias of the HV isolation circuit

	T0	reset	iso1	iso2
isolation	0	0	V_{DD}	V_{DD}
read (not reset)	V_{DD}	0	= BL	= BL
reset state	V_{DD}	V_{DD}	0	0

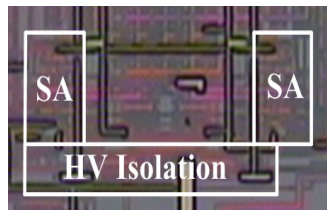


Fig. 7 The die microphotograph

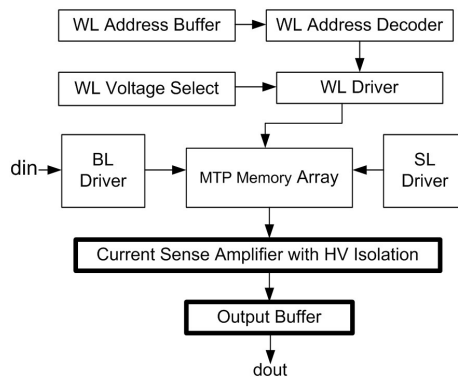


Fig. 2 The architecture to control the MTP array

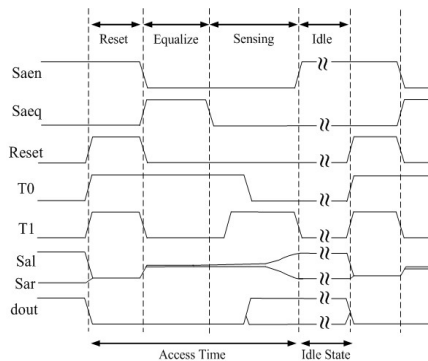


Fig. 5 The timing diagram of the SA with HV isolation and the output buffer

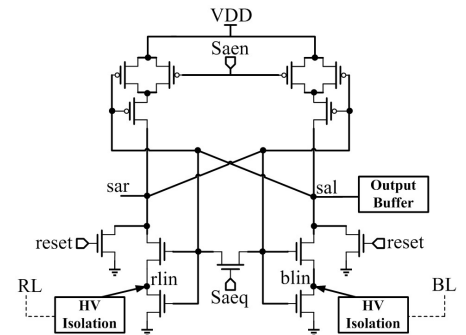


Fig. 3 The proposed current SA

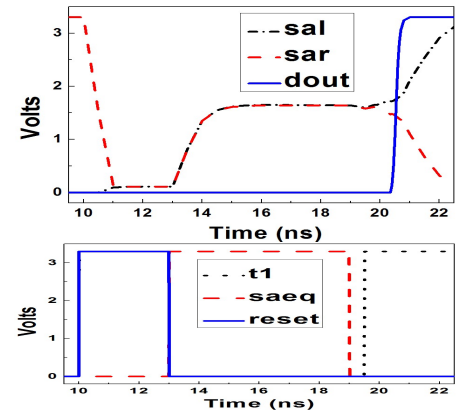


Fig. 6 Waveforms of the proposed SA

TABLE III. Comparison of SA's

	[6]	[7]	[8]	This work
AT (ns)	NA	NA	26	11(sim) 13(meas)
SDT (ns)	1.85	1.9	NA	1.4~1.8
SC (μ A)	NA	8~20	0.1~0.2	2~3
HV isolation	NO	NO	NO	YES

(sim:simulation, mea:measurement)
(AT: access time; SC: sensing current;
SDT:sensing delay time)

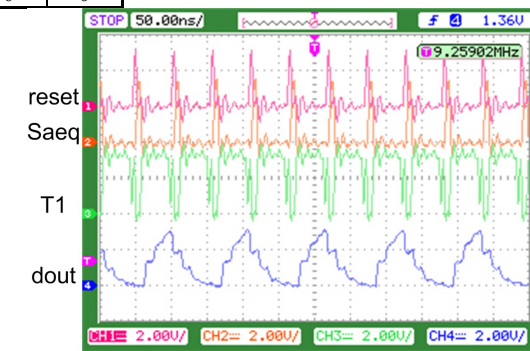


Fig. 8 The waveforms of the consecutive read operations from different MTP memory cells