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Emulation of High Frequency Substrate Noise in CMOS Digital Circuits with Effects of Adjusting Clock Skew

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Abstract

A digital noise emulator is based upon the capacitor charging modeling and generates power noises expected in a CMOS digital integrated circuit with skews among clock domains. An off-chip near magnetic field sensor indirectly characterizes the distribution of timings and the adjustability of skews in the on-chip digital circuit. An on-chip noise monitor captures power noise waveforms in a silicon substrate and evaluates noise frequency components in a wide frequency bandwidth. A 65 nm CMOS prototype clearly demonstrated the tradeoffs between skew adjustment and power noise suppression. Power noise emulated at 125 MHz exhibits the enhancements of high-order harmonic components after de-skewing with the timing resolution of 40 ps, as is specifically seen in more than 10 dB enlargement of the substrate noise component at 2.1 GHz.

1. Introduction

A single chip integration of radio-frequency (RF) circuits and digital signal processors has evolved with the advancements of CMOS technologies. The latest mobile wireless terminal is compliant with long-term evolution (LTE) standards and exhibits the high sensitivity for incoming weak signals as low as -100 dBm in the frequency band of 2.1 GHz (Band 1) [1]. A huge computation capacity is required in the digital backend processing for high-speed and broadband wireless channels where digital data are encoded on multiple carrier frequencies. On-chip power noise coupling through the common silicon substrate, often called substrate noise, is an obvious obstacle to meet these requirements in a future single chip solution. This paper presents the emulation of power noise in CMOS digital circuits targeting such high-capacity signal processing and off-chip and on-chip noise measurements for the characterization of power noises.

2. Noise Emulator

An on-chip digital noise emulator of Fig. 1 embodies the capacitor charging modeling [2] and produces power current as to be consumed in the operation of CMOS digital circuits under design. The power current flows through the impedance network of a power delivery system and appear as power noise. The emulator is consisted of eight noise generation blocks. Each block has a local clock buffer with de-skew function and an array of switched capacitor cells with programmable capacitance. The capacitor cell is switched by the local clock signal and connected to power nodes for consuming charges proportional to the programmed capacitance. The successive charging of capacitor cells consumes power current as is occurred equivalently in general CMOS digital circuits.

Power current flows in power traces on a printed circuit board and changes the near magnetic field. This is off-chip measured by a magnetic probe (MP), as shown in Fig. 2. The power current simultaneously creates voltage variations on power nodes within the emulator as well as on a silicon substrate. On-chip monitor (OCM) captures noise waveforms at various locations within the chip.

3. Experimental Results

Power current waveforms of the digital noise emulator are measured by MP as in Fig. 3. When a single noise generation block consumes charges, a large peak follows in power current. Since waveforms are synchronously captured against the universal clock signal of the emulator, the time difference between the clock edge and the peak in power current gives the internal skew, T_{skw}. The skews among eight blocks are measured as in Fig. 4(a) and show static distribution among the blocks with the span of 0.8 ns. A 7-bit delay generator is embedded in a local clock buffer and used for de-skewing at each block. The delay is measured similarly from the waveforms for delay codes obtained by MP, as plotted in Fig. 4(b). The range of 5 ns is linearly covered with the de-skew step of 40 ps. The distributed skews are leveled out by properly chosen delay codes among the blocks.

Power noise is generated at 125 MHz by the noise emulator, with and without de-skewing among the eight blocks. Substrate noise waveforms were on-chip measured by OCM and given in Fig. 5. Noise peaks are shaped substantially keen and impulse-like after de-skewing, and their regular appearance leads to high-order harmonic components. The frequency components are compared in Fig. 6 and specially exhibit more than 10 dB enlargements in the frequency band of 2.1 GHz. It is therefore shown that the operation of CMOS digital circuits even at the baseband frequencies can potentially interfere with RF signal processing in the narrow-bandwidth at the frequency of interest.

4. Conclusion

Power noise emulation of CMOS digital circuits was successfully demonstrated at 125 MHz and exhibited substrate noise components within the RF bandwidth at 2.1 GHz. While the finer de-skewing among clock domains is requested for achieving dense and high computation capacity, the intentional insertion of skews could be a remedy for suppressing power and substrate noise. These tradeoffs can be tested by the power noise emulator and to be balanced in the design of CMOS digital circuits.

Acknowledgments
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References

[1] The 3GPP, http://www.3gpp.org/
[2] K. Yoshikawa, et al. *IEEE EMC Compo.*, pp. 76-81, 2011.

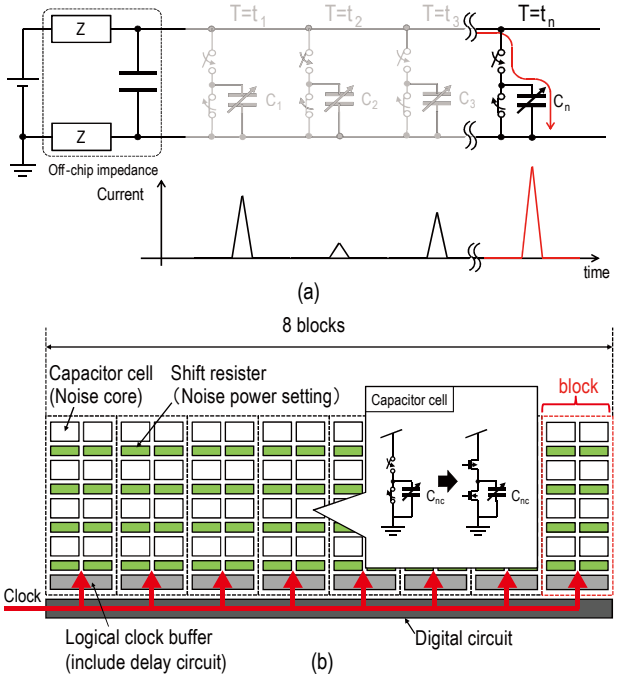

Fig. 1: On-chip noise emulator. (a) TSDPC model[2] (b) outline.

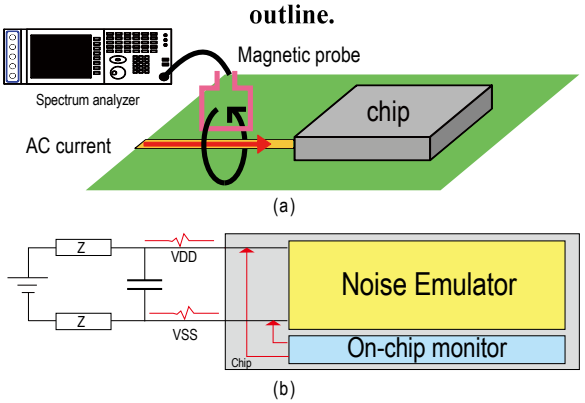

Fig. 2: (a) Off-chip and (b) on-chip noise measurements.

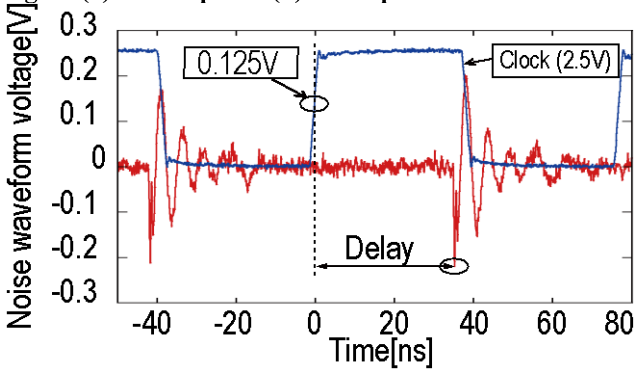

Fig. 3: Delay measurements using off-chip near magnetic field sensing.

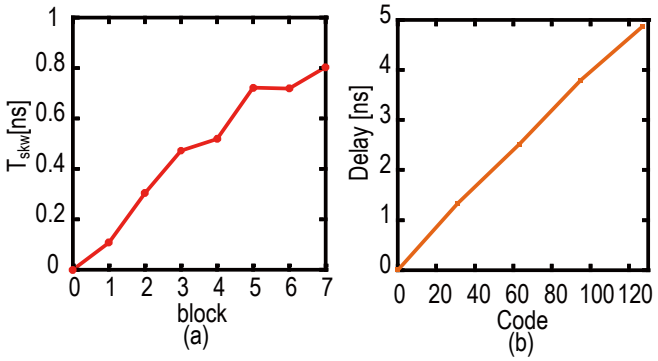

Fig. 4: (a) Distribution of timing difference among clock domains, and (b) skew adjustability with 7 bit codes.

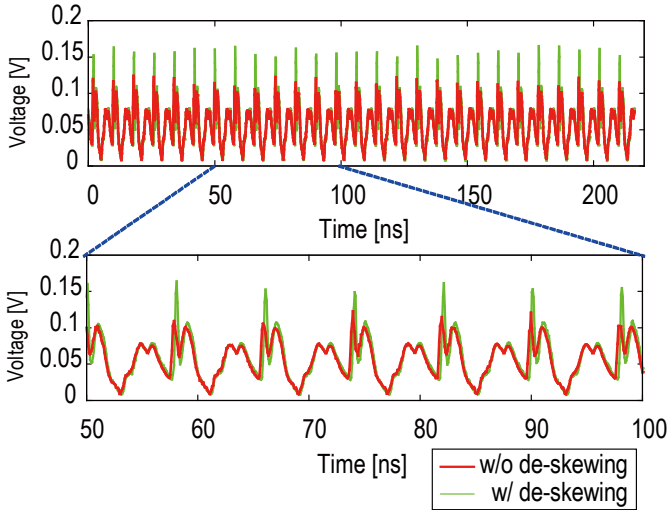

Fig. 5: On-chip substrate noise waveforms with and without skew adjustment.

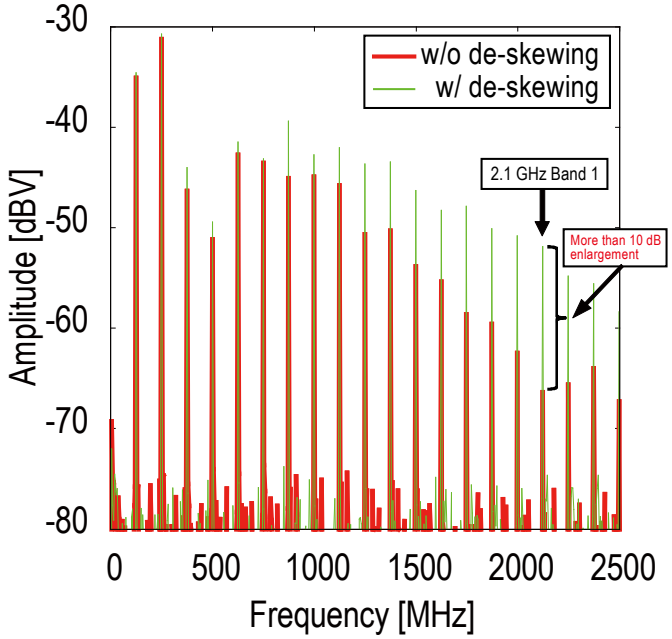

Fig. 6: On-chip substrate noise frequency components and high-order harmonics within 2.1 GHz band.