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High Power and High Q Spiral Inductors using TSV Processes

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Abstract

In this paper, a high aspect ratio metal can be made by using standard TSV process and high Q inductors are realized by using the technology. The fabricated inductor has 60 μm signal height and its Q factor is more than 30 at 2 GHz. As a result, Q factor of the TSV inductor is depend on signal spacing rather than signal width. The peak Q factor is maximized when the signal spacing is increased.

1. Introduction

In many RF-IC modules, spiral inductors are essential elements and their performances are important to RF circuits such as RF chokes, matching networks, VCOs, and various passive filters. Especially, because most monolithic RF-ICs have been used for wireless communications, the performance of the inductor are interested at 1~5 GHz.

The performance of the inductor is estimated by using quality factor (Q). At Q-rising region or low frequency regions, Q factor is depended on the ratio between the series inductance and resistance of the inductor ($Q_{DC}=\omega L/R$) [1]. Therefore, it is needed to reduce the resistance of the inductor to make high Q inductors at low-frequency. Increasing the metal thickness is the most efficient way to increase the Q factor in the low frequency regions. From this perspective, several methods have been studied in order to increase metal thickness, such as using electroplating [2] or using multi metal layers. Some papers have announced thick metal structures using dielectric-core [3]. The results of the papers show that a thick metal is very effective to improve Q factor. However, there are two problems to integrate thick spiral inductors. First, it is not easy to make high aspect ratio patterns. Generally, common photoresist can make a 1:1 ratio of pattern maximally, so the size of the inductor should be expanded to increase the metal thickness. Second, the thick metal structure make hard to package the devices and also it increase the thickness of the final packages.

In this paper, a new embedded spiral inductor is introduced to overcome the problems of the integrated thick spiral inductors. This inductor can be made with conventional TSV (Through Silicon Via) processes. Fig.1 shows the structures of the proposed spiral inductor. For various design parameters, the inductor was fabricated and their Q factors are analyzed.

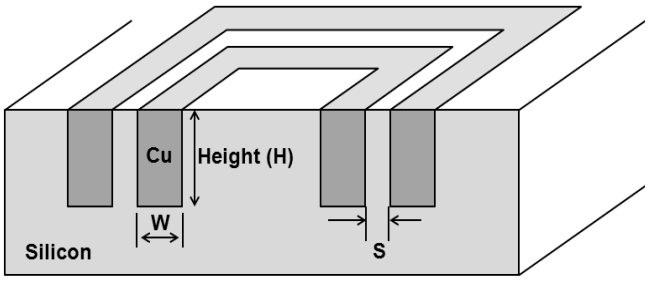

Fig. 1. Schematic of the TSV inductor

2. Fabrication Processes and Results

Fig. 1 shows the design structure of the TSV inductor. As shown in this figure, the metal thickness is determined from the depths (H) of silicon trench and it is embedded in the silicon. Signal width and spacing are defied as W and S respectively.

Fig. 2(a)~(d) show fabrication procedures of the inductor. The substrate was a 2000 Ω HRS (High Resistivity Silicon) and a deep RIE process was used to make fine spiral trench. The minimum signal width and spacing was 10μm respectively and the depth of the trench was 60μm. To fill the trench, copper electroplating method was used and planarization process was done after fully filling the trench. SU-8 epoxy was used as an isolation layer of the inductor. Fig. 2(e) and (d) show the photographs of the fabricated inductor. In this figure, signal width and spacing are 20 μm respectively and the back-side of the inductor was grinded to minimize substrate RF losses.

Fig. 2 shows the measured results of the inductor. ID means inner diameters of the inductor. For various turns (N), Q factors and series inductance (L) are shown in Fig. 2(a). The N=2.5 TSV inductor shows the Q_{Max}=34 at 2.5 GHz and its series inductance is 2 nH. Fig. 2(b) shows the Q and L for various signal width. As shown in this figure, there were few changes of Q and L in signal width variation. Fig. 2(c) shows the Q and L for various signal spacing. This graph shows the Q of the TSV inductor is very dependent on the signal spacing. Although series inductance is same, the Q factor was greatly improved (more than 37%) when the spacing was changed from 10 μm to 20 μm. The reason of the Q improvement is decrease of parasitic capacitance between signal lines where the silicon (ε_r=11.9) makes large stray capacitance.

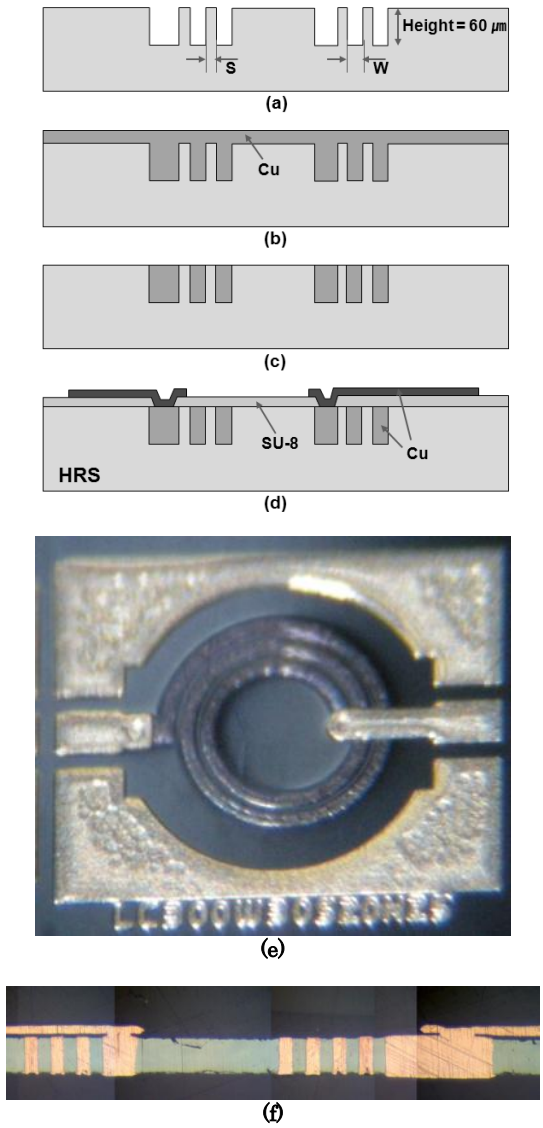

Fig. 2. Fabrication procedures and photographs of the TSV inductor. (a) Deep RIE etching. (b) Cu filling. (c) Planarization process. (d) Inner line interconnection. (e) Fabricated TSV inductor (plane). (f) Cross-section of the inductor.

3. Conclusions

A high-Q spiral inductor was made by using standard TSV process. This inductor has very thick signal height more than 60μm, so it can be used for high power devices or high performance RF circuits. As a result, the Q factor of the TSV inductor was very dependent on the signal spacing rather than signal width. The fabricated TSV inductor had the largest Q factor when the spacing is 20 μm and its value was 30 at 2 GHz.

Acknowledgements

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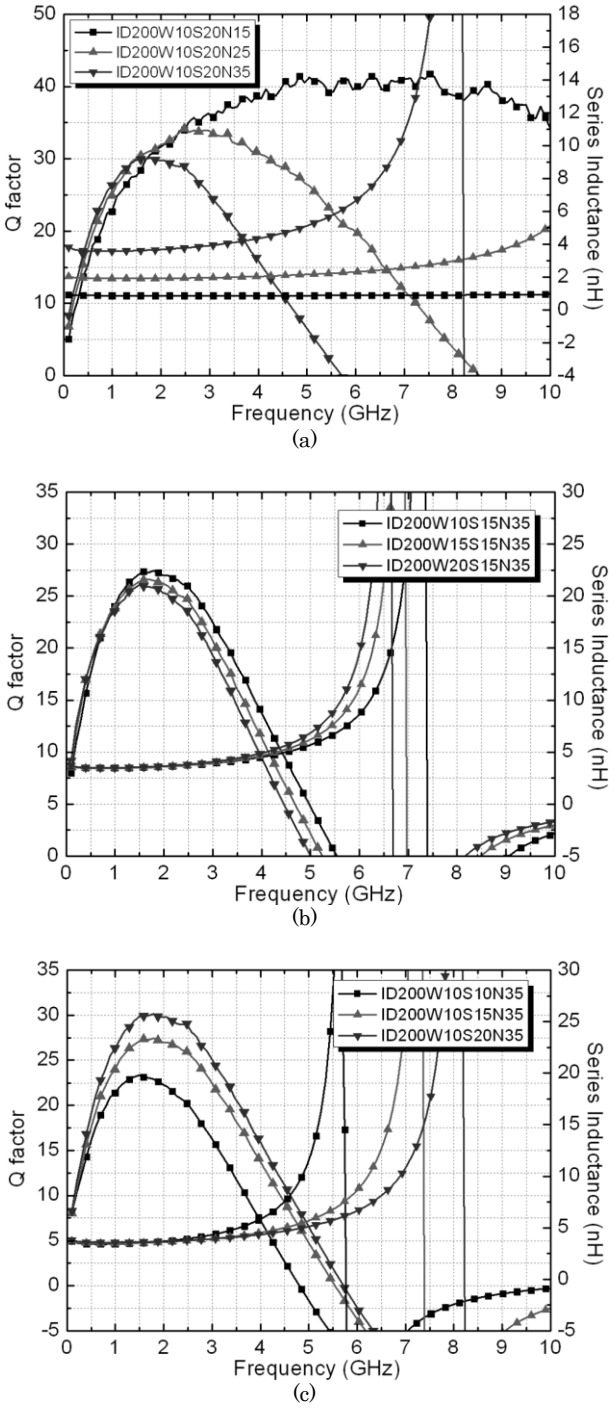

Fig. 2. Measured Q and L of the TSV inductor. (a) Various turns (N=1.5, 2.5, 3.5) (b) Various signal width (W=10, 15, 20 ㎛). (c) Various signal spacing (S=10, 15, 20 ㎛)

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