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Design Optimization Methodology for Ultra Low Power Analog Circuits using Intuitive Inversion-level and Saturation-level Parameters

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Abstract

An intuitive and comprehensive design optimization methodology by means of inversion-level and saturation -level parameters is proposed for ultra low power, low voltage and high performance analog circuits with mixing strong, moderate and week inversion MOSTs' operations.

1. Introduction

Enabling ultra low power and low voltage analog circuits with high performance is an urgent issue for battery-operated portable equipments and implantable biomedical devices. Several attempts have been studied and proposed in the light of one-equation MOST(MOS-Transistor)'s models[1,2] and analog circuits design methodologies[3,4,5]. However each one-equation model has both strong and weak points and the proposed design methodologies based on those models are very useful but not always intuitive or comprehensive in searching the best design solution for various application specifications.

This paper presents an intuitive and comprehensive design analysis/optimization methodology especially aiming for ultra low power, low voltage and high performance analog circuits.

2. Synthesized Charge-based MOST Model

There are two main charge-based one-equation MOST's models called as EKV[1] and ACM[2]. The EKV model is the first model that gave a novel perspective for MOST's one-equation expression including both strong/weak inversions and linear/saturation modes by introducing a new parameter of 'Inversion Coefficient' (*IC*), but unfortunately the equation which combines *IC* with the gate voltage (*Vg*) is an artificial mathematical approximation and is not accurate in moderate inversion region. On the other hand, the ACM model showed the exact physical equation between *IC* and the gate voltage in an implicit function form for the first time, but their defined *IC* is not identical to EKV's. Afterward EKV's *IC* was proved to be a well-defined center parameter for inversion mode criteria[6]. We adopt the synthesized model composed of EKV's basic concepts and ACM's physical expressions.

Fig. 1 shows the concept of EKV's *IC*, called as i-level(***i***) in this paper. The i-level is the ratio of drain current divided by the threshold voltage current, and provides an intuitive numerical representation of the MOS inversion level. Strong inversion corresponds to $i > 10$, while weak inversion corresponds to $i < 0.1$. For $0.1 < i < 10$, MOST is operating in moderate inversion.

Fig. 2 shows hand calculation fitting comparison between conventional model and this new i-level model. This model also reproduces temperature-dependent characteristics that is indispensable for analog circuits margin/stability analysis.

3. Intuitive Analog-Circuits Optimization Methodology

The key concept of our design methodology is to start from i-level design by using some i-level equations derived from application specification, circuits stability and other constraints. For this purpose, not only MOST characteristics but also system characteristics are described by i-level as shown in Fig.3. Table1 shows basic nine i-level expressions for MOST. It should be noted that while item6-9 in Table1 contain process parameters like Pelgrom coefficient of *Avt* or MOST size, item1-5 are not dependent on those process or size parameters.

There are two universal characteristics in relation to i-level. Fig.4 (right) shows a universal characteristics of saturation voltage (*Vdsat*). The saturation region exists in all inversions and lower saturation voltage in moderate and weak inversions is a valued benefit for low supply voltage circuits. Fig.5 shows another universal characteristics of gm/Id which represents not only current drivability but also variability. The gm/Id curves indicate optimum design size for variability (Table1 item 6) .

Our design methodology starts from i-level design using those universal characteristics, called as 'Universal design' step or '***i***-design'. This paper introduces a example of our design methodology for two stage Miller amplifier as shown in Fig.6. The following i-level equation for MOST *M1*/*M2* is derived from the stable phase margin requirement,

$$\sqrt{1+4\cdot i_1}+5\sqrt{1+4\cdot i_2}=\left(\frac{I_{total\_current}}{\omega_u\cdot 0.3C_L\cdot n\phi_T}-6\right) \qquad (1).$$

Fig.7(left) shows the solution zone for (i_1,i_2) under low total-current values in case of $\omega_u=100kHz$, $C_L=10pF$ and the phase margin>60 degree. When total current becomes less than $2\mu A$, the solution exists in moderate region. Fig.7(right) shows input common mode and output range using A values of $i_3=A3*i_1$, $i_5=A5*i_1$ and $i_4=A4*i_2$. A tradeoff relationship between total current and gain bandwidth is also derived as shown in Fig.8.

After the 'Universal Design' step, 'PDK-specific Design' step begins as shown in Fig.6 by utilizing item6-9 with process and size parameters in Table1. The final step is the simulation by EDA tool in full consideration of detailed parasitic capacitance attributed to MOST design size, while verifications are executed including the saturation test for each MOST operation point by using saturation-level criteria that is newly defined in this paper(Table1 item 3). Saturated operation of $Vd>Vdsat$(Table1 item4) corresponds to saturation-level***(s)***>1.

4. Conclusion

An intuitive design optimization methodology for analog circuits is proposed. This methodology also opens the way to a comprehensive design approach for analog circuits with mixing strong, moderate and week inversion MOSTs' operations.

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Table 1 ***i*** (inversion level)-based MOST Parameter Set
(<>: *PDK(Process Design Kit)-parameter*)

	Transistor items	New model expression	Parameter
	definition I_Z	$I_Z \equiv 2n\phi_T^2 \cdot \mu C_{ox}\left(\frac{W}{L}\right) = 2n\phi_T^2 \cdot \beta \quad \left\{n \approx 1.3 \quad ,\phi_T = \frac{kT}{q}\right\}$	L,W <μC_{ox}>
	definition V_{th}	$V_{th} \equiv V_G\left(@\, i = \frac{3}{4} \approx 1 \quad or \quad I_D = \frac{3}{4} \cdot I_Z\right)$	—
1	all inversion equation	$\frac{V_G - V_{th}}{n} - V_S = \phi_T\left[\sqrt{1+4\cdot i} - 2 + \log_e\left(\sqrt{1+4\cdot i} - 1\right)\right]$	i, V_G, V_S
2	inversion-level	$i \equiv \frac{I_D}{I_Z}$ $\left\{\begin{array}{lll} weak & mod erate & strong \\ i<0.1 & 0.1 \le i < 10 & 10 < i \end{array}\right\}$	i
3	saturation-level	$s \equiv \frac{2}{100} \cdot exp\left[\frac{V_{DS}}{\phi_T} + 1 - \sqrt{1+4\cdot i}\right]$ $\left\{\begin{array}{ll} linear & saturation \\ s \le 1 & 1 < s \end{array}\right\}$	i, V_{DS}
4	saturation voltage	$V_{Dsat} = \phi_T\left[\sqrt{1+4\cdot i} + 3\right]$	i
5	conductance (gate)	$g_m \equiv \frac{\partial I_D}{\partial V_G} = \frac{2I_D}{n\phi_T}\left[\frac{1}{\sqrt{1+4\cdot i}+1}\right]$	i, I_D
6	resistance (drain)	$r_0 \equiv \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} = \left(\frac{I_D}{V_A}\right)^{-1} = \frac{V_0 \cdot i^{1-\alpha}}{I_D}$ $\left\{V_A \approx V_0 \cdot i^{(1-\alpha)}\right\}$	i, I_D <V_A>
7	drain current variety	$\frac{\Delta I_D}{I_D} = \frac{A_{VT}}{\sqrt{WL}}\left(\frac{g_m}{I_D}\right) = \frac{A_{VT}}{\sqrt{WL}} \cdot \left(\frac{2}{n\phi_t}\right) \cdot \left[\frac{1}{\sqrt{1+4\cdot i}+1}\right]$	i, L, W <A_{VT}>
8	noise (thermal)	$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma \cdot n\phi_t \mu C_{ox}\left(\frac{W}{L}\right)\left(\sqrt{1+4\cdot i}-1\right)$	<μ> <C_{ox}>
	noise (flicker)	$\frac{\overline{v_n^2}}{\Delta f} = \frac{K1}{C_{ox}^2 \cdot WL}\left[\left(\frac{1+\sqrt{1+4\cdot i}}{2}\right)^2 \frac{\log_e(1+4\cdot i)}{4i}\right]$	<$K1$>
9	intrinsic transition frequency	$f_T = \frac{\mu\phi_t}{\pi L^2}\left(\sqrt{1+4\cdot i}-1\right)$	i, L <μ>

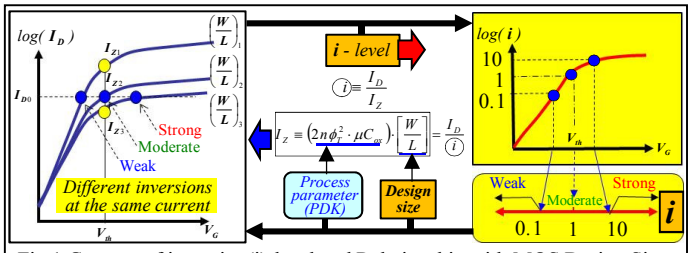

Fig.1 Concept of inversion(i)-level and Relationship with MOS Design Size

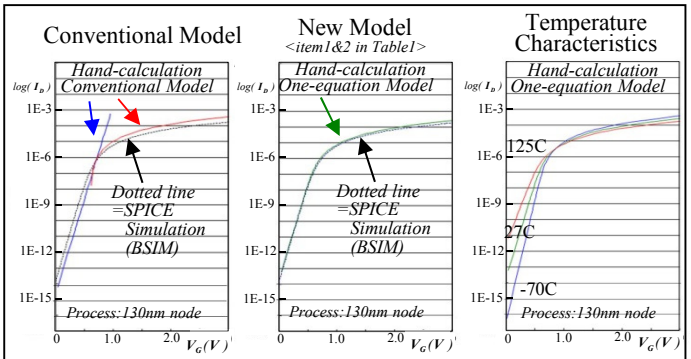

Fig.2 Model Fitting Accuracy and Temperature Dependent Characteristics

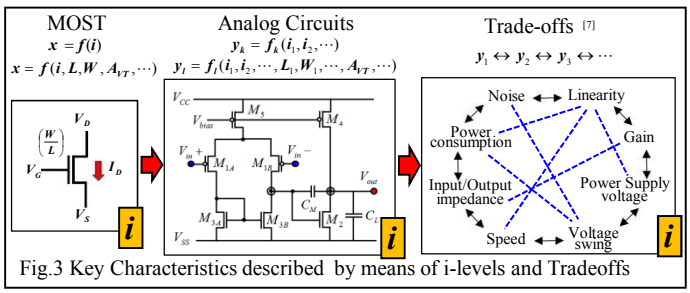

Fig.3 Key Characteristics described by means of i-levels and Tradeoffs

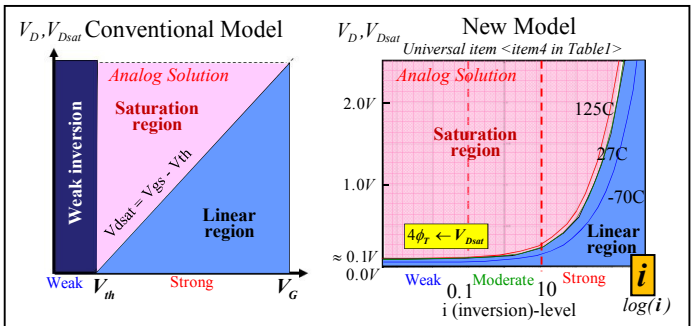

Fig.4 Vd-saturation Region of Conventional Model(left) and New Model(right)

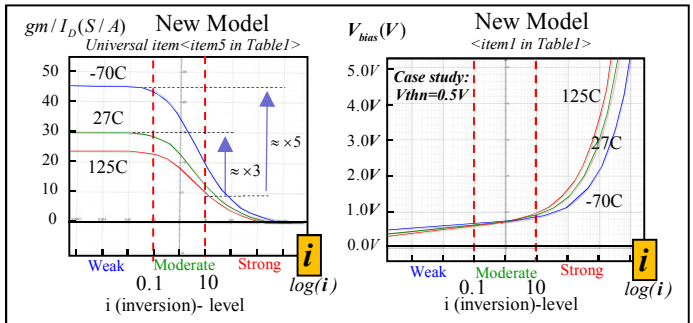

Fig.5 Temperature Dependent Characteristics for gm/Id(left) and Vbias(right)

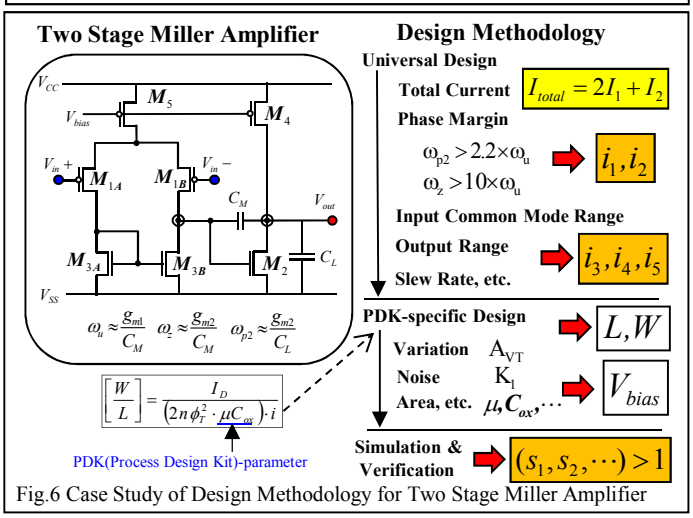

Fig.6 Case Study of Design Methodology for Two Stage Miller Amplifier

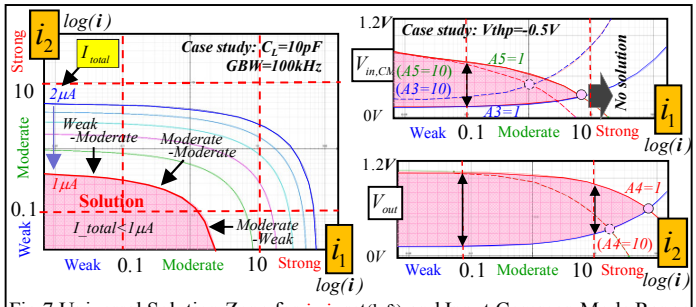

Fig.7 Universal Solution Zone for i_1-i_2 set(left) and Input Common Mode Range (right up) / Output Range(right down) for i_3=A3*i_1, i_5=A5*i_1 and i_4=A4*i_2 settings in case of Two Stage Miller Amplifier of 1μA Current and 1.2V Power Supply Voltage.

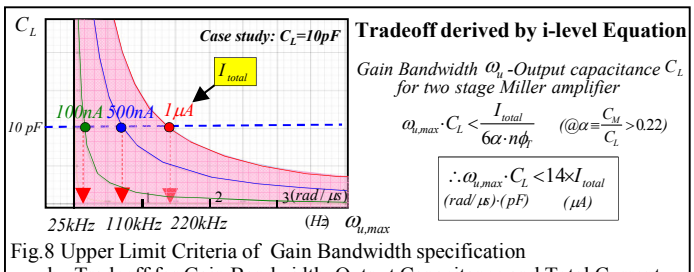

Fig.8 Upper Limit Criteria of Gain Bandwidth specification by Tradeoff for Gain Bandwidth, Output Capacitance and Total Current