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Microwave Performance of $In_{0.25}Ga_{0.75}As$ MOSFET with an InGaP interfacial layer*

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Abstract

High performance buried $In_{0.25}Ga_{0.75}As$ channel metal-oxide-semiconductor field-effect transistor (MOSFET) with Si-doped $In_{0.49}Ga_{0.51}P$ interfacial layer has been fabricated. A 1-μm-gate length $In_{0.25}Ga_{0.75}As$ MOSFET with InGaP interfacial layer and 8 nm Al_2O_3 dielectric shows a short circuit current gain cutoff frequency of 16.7 GHz and a maximum oscillation frequency of 52 GHz.

1. Introduction

III-V compound semiconductor such as $In_xGa_{1-x}As$ have attracted much more attention as a new channel alternative of MOSFET because of its high bulk electron mobility and low electron effective mass[1],and high electron mobility III-V MOSFET is potential attractive devices for future application in diverse fields including digital[2], analog/mixed-signal[3] and radio-frequency[4]. Remarkable microwave characteristics are essential for their RF applications. A record high f_T of 244 GHz and f_{max} of 292 GHz has been reported for a L_g=55 nm InGaAs surface channel MOSFET using H_fO_2 and Al_2O_3 as gate dielectrics [5]. In this letter, it is the first time that a buried channel $In_{0.25}Ga_{0.75}As$ MOSFET with Si-doped $In_{0.49}Ga_{0.51}P$ interfacial layer and 8 nm Al_2O_3 as gate oxide fabricated on GaAs substrate for radio frequency application was reported.

2. Device structure and experimental procedure

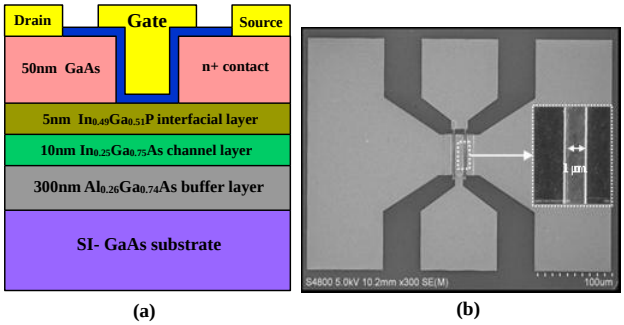

Fig.1 (a) Schematic cross-section of $In_{0.25}Ga_{0.75}As$ MOSFET; (b) The SEM graph of the MOSFET device

Fig. 1(a) shows the cross-section of this $In_{0.25}Ga_{0.75}As$ MOSFET. The MOSFET structure consisted of (from bottom to top), a 300-nm-thick $Al_{0.28}Ga_{0.72}As$ buffer layer, a 10 nm $In_{0.25}Ga_{0.75}As$ strained quantum well channel layer, a 5 nm $In_{0.49}Ga_{0.51}P$ interfacial layer, and a n^+ contact layer which is a 50 nm GaAs cap layer. Fig. 1(b) shows the top-view scanning electron microscope (SEM) micrograph of completed device.

The technological process of InGaAs MOSFET as following: Device isolation is achieved by mesh etching; Gate recess is next defined by wet etching; Diluted hydrochloric acid cleaning and ammonia based surface preparation; A 8 nm Al_2O_3 was deposited by atomic layer deposited (ALD) as gate oxide; Post deposition annealing at 400 ℃ in nitrogen (N_2) ambient; Gate electrode is realized by electron beam evaporation of Ni/Au and a lift off process; Ni/Ge/Au/Ge/Ni/Au source and drain (S/D) ohmic contacts are deposited; Rapid thermal annealing (RTA) process at 270 ℃ for 3 min in a N_2 ambient.

3. Results and discussion

Fig.2 shows output characteristics of a 1-μm-gate length MOSFET with gate voltage from -2 V to 3 V in steps of 500 mV, exhibiting maximum drain current of 350 mA/mm obtained at V_{gs}=3 V and V_{ds}=2.5 V. The transfer characteristic of the MOSFET are shown in Fig.3, the peak extrinsic transconductance of 140 mS/mm is achieved at V_{ds}=2.5 V. The effective electron mobility of InGaAs channel has been characterized by using split-CV method. As shown in Fig.4, the InGaAs nMOSFET exhibited higher effective electron mobility compared with corresponding device without InGaP barrier layer. The peak electron mobility of InGaAs channel is 1266 cm^2/Vs due to the InGaP interfacial layer.

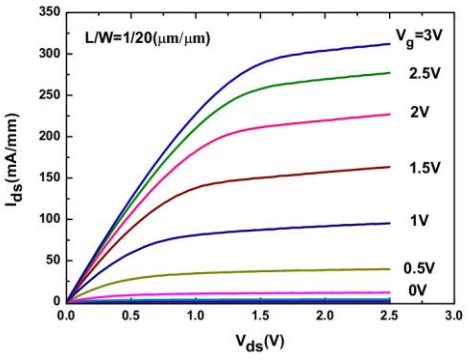

Fig.2 Measured drain current density versus drain-to-source voltage of the MOSFET

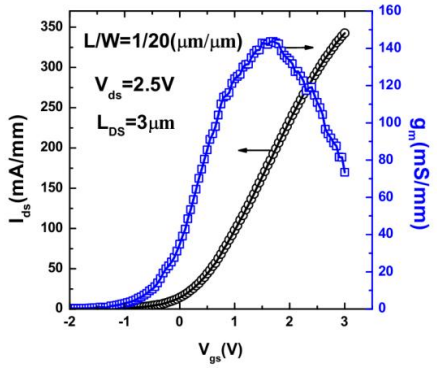

Fig.3 The transfer and transconductance characteristics of the InGaAs MOSFET with InGaP interfacial layer

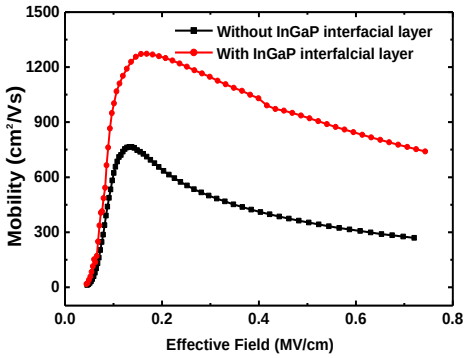

Fig.4 The effective channel mobility versus effective field of the MOSFET with and without InGaP interfacial layer

Microwave on-wafer S-parameter measurements of up to 20 GHz were carried out at room temperature. As shown in Fig.5, for a L_g=1 μm MOSFET, biasing at V_{ds}=2.5 V and V_{gs}=3 V, after de-embedding the parasitic effects from open-short dummy structures, peak unity current gain cutoff frequency (f_T) of 16.7 GHz was achieved from current gain (h_{21}) curve, meanwhile the maximum oscillation frequency (f_{max}) of 52 GHz was extracted by extrapolation of Mason's unilateral power gain. In addition, Fig.6 shows a wide range bias dependence of the measured f_T with gate voltage from 0 V to 3 V in steps of 0.2 V.

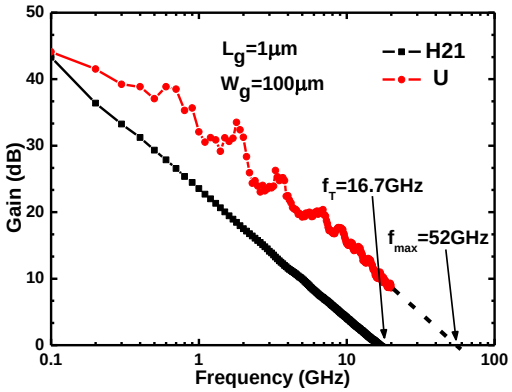

Fig.5 Current gain and unilateral power gain versus frequency for the 1μm×100μm MOSFET at V_{gs}=3 V and V_{ds}=2.5 V

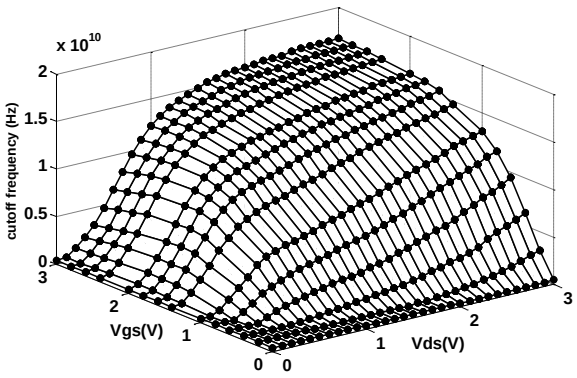

Fig.7 Three-dimensional plots of f_T versus gate and drain voltages of the MOSFET

4. Conclusion

In summary, we have demonstrated a buried channel $In_{0.25}Ga_{0.75}As$ MOSFET on GaAs substrates with $In_{0.49}Ga_{0.51}P$ interfacial layer. The proposed $In_{0.25}Ga_{0.75}As$ MOSFET shows a high drive current density and transconductance. The 1 μm gate-length device exhibits a f_T of 16.7 GHz and an f_{max} of 52 GHz.The simulated f_T was also presented. All the results indicate that $In_{0.25}Ga_{0.75}As$ MOSFET with InGaP interfacial layer is of great potential for microwave applications.

Acknowledgment

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