PS-6-18

Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp176-177

On the electrical characteristics of the atomic layer deposition $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOSCAPs with various annealing processes

Quang-Ho Luc[1], Edward Yi Chang[1, 2*],Hai-Dang Trinh[1], Hong-Quan Nguyen[1], Binh-Tinh Tran[1], Yueh-Chin Lin[1] and Huy-Binh Do[1]

[1] Department of Materials Science and Engineering, National Chiao Tung University
1001 University Road, Hsinchu 300, Taiwan
[2] Department of Electronics Engineering, National Chiao Tung University
1001 University Road, Hsinchu 300, Taiwan
*E-mail: edc@mail.nctu.edu.tw

Abstract

We investigate the impact of different annealing processes on the electrical properties of $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$ structures. The post deposition annealing (PDA) and post metallization annealing (PMA) processes with different temperatures (250 – 400 °C) and ambient (N_2 and forming gas (FG)) are studied through capacitance-voltage (*C-V*), current-voltage (*J-V*), and the *Auger* depth profile analyses. The lower leakage current and better *C-V* behaviors are observed on the samples with high PDA temperature step. The root cause of leakage current is attributed to the out-diffusion of Pt into Al_2O_3 layer, rather than the oxide densification, which results in the electrical characteristics degradation at high annealing temperature. Moreover, the improvement on the Al_2O_3/InGaAs interfaces quality and leakage current with the PDA process for 5 minutes in FG at 400 °C certify the benefit of forming gas annealing.

1. Introduction

The continues downscaling of the metal oxide semiconductor field effect transistor (MOSFET) requires the integration of III-V compound semiconductor as high mobility channel to replace the conventional Si for future CMOS technology [1]. However, the nature poor interfacial quality of high-k/III-V still remains a big issue that inhibits the performance of devices [2]. In this article, we report the impact of different annealing processes with various annealing conditions on the electrical characteristics of ALD-$Al_2O_3/In_{0.53}Ga_{0.47}As$ structures. The benefit of forming gas annealing on the C-V behaviors can only be affirmed in the case of the high PDA temperature samples.. The degradation of C-V properties of the PMA samples due to the high leakage current is found to originate from the out-diffusion of metal gate into oxide layer.

2. Experimental

The wafers used in this study were solid source molecular beam epitaxy grown 100 nm n-$In_{0.53}Ga_{0.47}As$ layer (5×10^{17} /cm^3 doping) on n^+-InP substrates. Starting surfaces were degreased in acetone and isopropanol before the chemical treatment with HCl:H_2O (1:10) solution for 2 min. The samples were then loaded into Atomic Layer Deposition (ALD) chamber (Cambridge NanoTech Fiji-202 DCS) for ten cycles of TMA/N_2 (half an ALD cycle) followed by the growth of 85 cycles of Al_2O_3 films at 250 °C. After oxide deposition, two series of samples with different annealing processed were performed as described in table I.

Table I List of samples for annealing studies

Samples	PDA process	PMA process
i	**N/A**	**300°C in N_2 for 5 min**
ii	**N/A**	**350°C in N_2 for 5 min**
iii	**N/A**	**400°C in N_2 for 5 min**
iv	**N/A**	**400°C in FG for 5 min**
v	**400°C in N_2 for 5 min**	**250°C in N_2 for 30 sec**
vi	**400°C in FG for 5 min**	**250°C in N_2 for 30 sec**

After PDA process, the Pt gate metal and Au/Ge/Ni/Au back side ohmic contact were formed with electron beam evaporation followed by PMA process.

3. Results and discussion

The bidirectional C-V responses at 1 MHz of $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$ structures fabricated with various PDA and PMA processes are shown in Fig. 1.

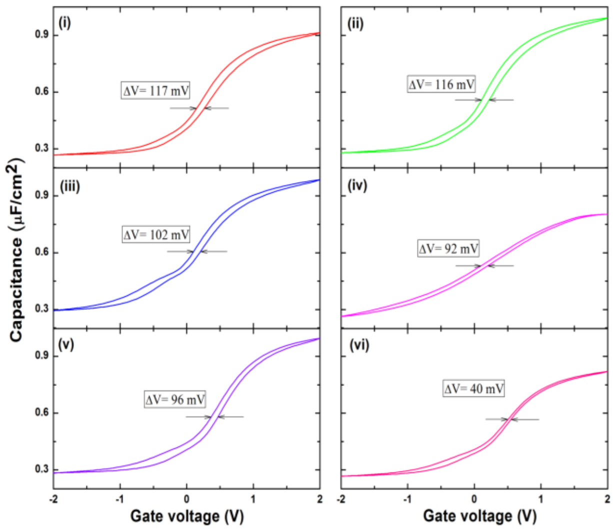

Fig.1. The bidirectional C-V response of samples (i), (ii), (iii), (iv), (v) and (vi)

Typically, annealing in FG always yields a greater reduction in hysteresis as compared to annealing in N_2 ambient. The hysteresis near flat band of samples annealed at 400 °C is smaller than that of samples annealed at lower temperatures. As can be seen form Fig. 1, it is apparent that PDA step is more effective than PMA step which is demonstrated by the better C-V properties of PDA samples. Sample (vi) reveals the smallest C-V hysteresis value of only 40mV illustrating a good interface quality, whereas, sample (iv) still has significant hysteresis value (~ 92 mV) after FG ambient treatment.

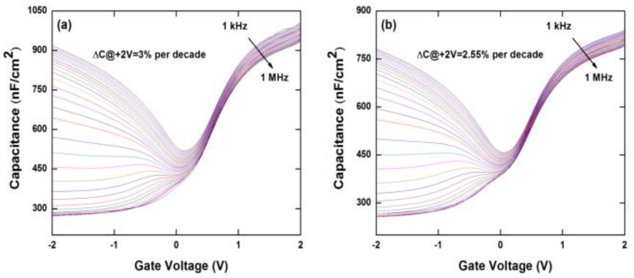

Fig.2. The multifrequency C-V curves of samples (v) and (vi)

Fig. 2 illustrates the multifrequency C-V response of sample (v) and (vi). Compare to sample (v), the C-V curves of sample (vi) clearly exhibit excellent electrical characteristics of C-V stretch-out, hysteresis and frequency dispersion (Fig. 2). These responses are characterized by clear accumulation/depletion regions and very close to true inversion behavior which implies that the minority carriers are nearly free from interfaces trapping. From Fig. 2b, a significant decrease of both border traps and interfaces states in sample (vi) are demonstrated by the small frequency dispersion value of 2.55% per decade at the accumulation region and almost disappearance of the weak inversion "bump". The interface trap densities at 0.2 eV below the conduction band edge (Ec) extracted by conductance method were 1.5×10^{12} $cm^{-2}eV^{-1}$ and 1.375×10^{12} $cm^{-2}eV^{-1}$ for sample (v) and (vi), respectively.

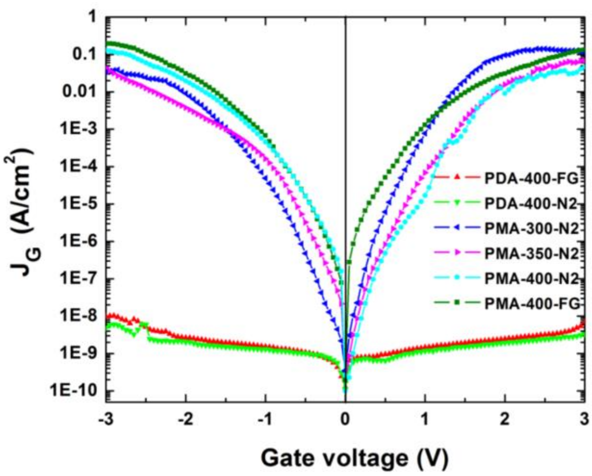

Fig.3. The leakage current density versus gate bias (J-V) of samples with various annealing processes

Fig. 3 clearly showed that leakage current density of PMA samples are approximately six orders of magnitude higher than that of PDA samples regardless of annealing ambient. The samples experienced PDA step exhibit low leakage currents in conjunction with the improvement of Al_2O_3/InGaAs interface and oxide qualities. These observations strongly suggested that the sequence of thermal treatment does have a pronounced influence on electrical properties of the structures.

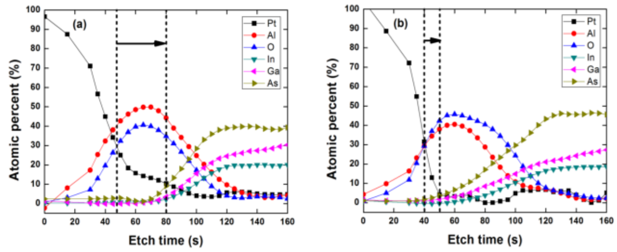

Fig.4. The Auger depth profiling analyses of (a) sample annealed after gate formation and (b) sample annealed before gate formation

Fig. 4 shows the *Auger* depth profiling analyses of PMA and PDA samples annealed at 400 °C. In conjunction with the *J-V* measurements, these results indicate that there is a strong diffusion of Pt into Al_2O_3 for the PMA sample which was not found in the PDA sample at the same annealing temperature. This trend confirms that the major effect of annealed thermal budget is an impulse to out-diffusion of Pt metal which leads to high leakage current.

4. Conclusions

In summary, we have presented the influence different of annealing processes on the interfacial properties of the Pt/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSCAPs. The root cause of high leakage current observed on the PMA step is originated from the out-diffusion of Pt into Al_2O_3 layer. The benefit of forming gas annealing can only be achieved in consequence of PDA step.

Acknowledgements

This work was supported by the NCTU-UCB I-RiCE Program and sponsored by the Taiwan National Science Council under Grant Number: NSC-102-2911-I-009-301.

References

[1] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz and M. Radosavljevic, IEEE Trans. Nanotechnology **4** (2005) 153.

[2] Y. Xuan, Y. Q. Wu and P. D. Ye, IEEE Electron Device Lett., **29** (2008) 294.