

Design of AlGaAs/InGaAs Heterojunction Tunneling Field-Effect Transistor for Low-Standby-Power and High-Performance Application

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1. Introduction

Increasing significance of power consumption in the nanoelectronic circuits calls for low standby power (LSTP) and low supply voltage (V_{DD}) operation have been required. Tunneling field-effect transistor (TFET) is a candidate with such capabilities due to excellent performance such as steep subthreshold swing (S) and low off-state current (I_{off}). Low on-state current (I_{on}) of silicon (Si) TFETs can be overcome by employing compound materials, high- κ dielectrics, and novel structuring [1-3]. Compound heterojunction TFETs with wide range of energy bandgap (E_g) can be designed to have higher I_{on} than conventional MOSFETs at a low V_{DD} . Also, TFETs should have a sharp band bending between source and channel to minimize the effective tunneling barrier width (W_T), since thinner W_T greatly improves both I_{on} and S . Compound semiconductors with various electron affinity (EA) and E_g have more chances to construct heterojunctions having steeper band bending [4]. AlGaAs/InGaAs can be also a candidate for hetero-structuring in TFETs. Even though GaAs has a larger energy bandgap ($E_g = 1.42$ eV) than that of Si ($E_g = 1.12$ eV), $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ heterojunction can form steep interfacial band bending by a large difference between EAs. In this work, we propose and characterize a TFET with $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_{1-y}\text{Ga}_y\text{As}$ heterojunction achieving LSTP and high performance (HP) operations at as low V_{DD} as 0.5 V. 3-dimensional (3D) device simulations were performed for an optimal device design in terms of I_{on} , I_{off} , S , threshold voltage (V_{th}), and intrinsic delay time (τ).

2. Device Design and Performances

The design and characterization have been performed by device simulations (both TCAD and ATLAS) activating multiple models including non-local band-to-band tunneling (BBT) (spatial variations are taken into account) and trap-assisted tunneling (TAT) models for higher accuracy [5–6]. In incorporating higher Al and lower In fractions in $\text{Al}_x\text{Ga}_{1-x}\text{As}$ and $\text{In}_y\text{Ga}_{1-y}\text{As}$, respectively, they have a small lattice mismatch (for $x = 0.7$ and $y = 0.2$, respective lattice constants are 5.734 Å, 5.659 Å). In device simulations, doping concentrations of p^+ AlGaAs/ p^- InGaAs/ n^+ InGaAs (source/channel/drain) are 5×10^{19} cm⁻³, 1×10^{16} cm⁻³, and 1×10^{19} cm⁻³, in sequence; The channel length, radius, and gate oxide thickness of a designed

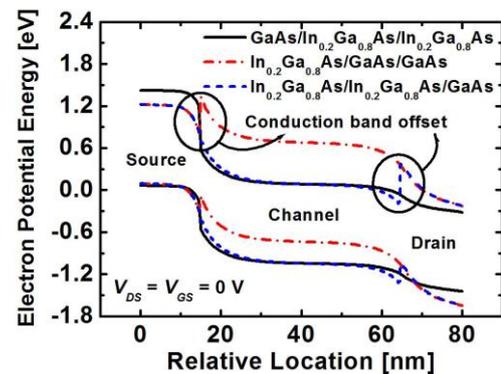


Fig. 1 Energy-band diagrams of TFETs having GaAs/ $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ heterojunctions.

device structure are 50 nm, 10 nm, and 3 nm, respectively; the workfunction of gate metal (Φ_m) was set to 4.75 eV.

Fig. 1 shows energy-band diagrams of TFETs having GaAs/ $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ heterojunctions of various arrangements. In case of $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ heterojunction TFET, the difference between EAs of $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ and GaAs builds a discontinuous potential barrier seen either from source to channel (red dotted line) or from channel to drain (blue one) due to the conduction band offset which degrades I_{on} . On the other hand, when GaAs/ $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ heterojunction is deployed in the source-to-channel interface, a smooth conduction band is obtained due to smaller EA of GaAs.

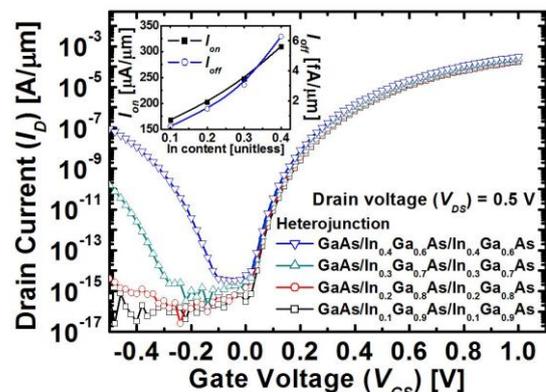


Fig. 2 Transfer curves of GaAs/ $\text{In}_y\text{Ga}_{1-y}\text{As}$ heterojunction TFETs.

Fig. 2 shows the drain current (I_D) vs. gate voltage (V_{GS}) transfer curves of GaAs/ $\text{In}_y\text{Ga}_{1-y}\text{As}$ heterojunction TFETs.

As In content in $\text{In}_y\text{Ga}_{1-y}\text{As}$ increases, I_{on} prominently increases up to $300 \mu\text{A}/\mu\text{m}$ as depicted in the inset of Fig. 2, while I_{off} shows only a small amount of increase in a range of a few femto-amperes (fA). I_{on} and I_{off} are defined as the drain current at $V_{GS} = 1 \text{ V}$ and onset V_{GS} , both at $V_{DS} = 0.5 \text{ V}$, respectively. As In content of $\text{In}_y\text{Ga}_{1-y}\text{As}$ goes up to 0.3, a significant ambipolar behavior is observed due to the narrow bandgap initiating leakage current at the drain end. For this reason, a low enough In content of 0.2 is maintained in the InGaAs channel and drain for optimal design.

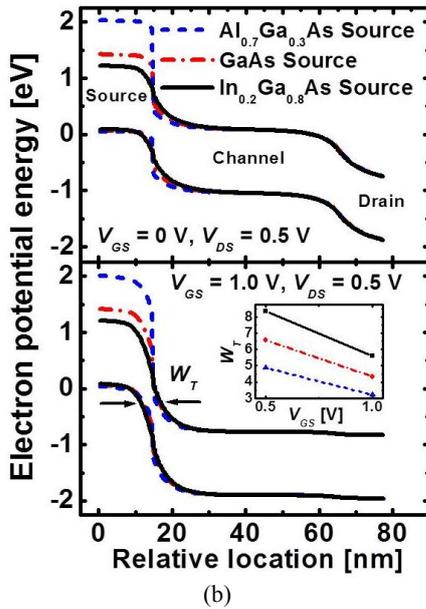
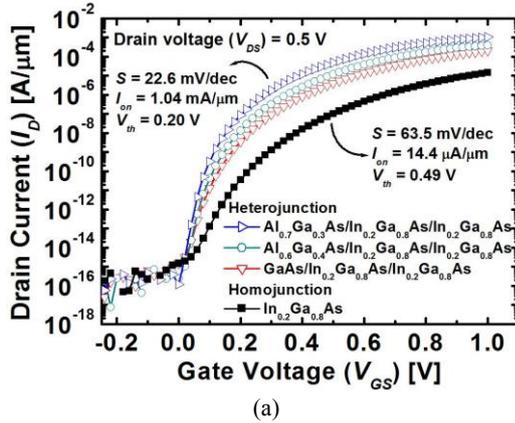


Fig. 3 DC characteristics. (a) I_D - V_{GS} transfer curves. (b) Energy-band diagram at different source material.

Fig. 3 demonstrates direct-current (DC) characteristics of $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}$ heterojunction TFETs with different source materials. $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ TFET shows improved I_{on} and S (average slope between two points of onset V_{GS} and $V_{th} = [V_{GS} \text{ at } I_D = 10^{-7} \text{ A}/\mu\text{m}]$), and $V_{th} = 0.2 \text{ V}$ suitable to LSTP operation as confirmed in Fig. 3(a). The large difference between EAs of $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}$ (source) and $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ (channel) thins W_T and eventually improves I_{on} , as proven in a more graphical manner by Fig. 3(b).

Fig. 4 depicts the intrinsic delay time (τ) as a function of V_{GS} at $V_{DS} = 0.5 \text{ V}$ ($\tau = C_{gg} \cdot V_{DD}/I_{on}$), where V_{DD} is the

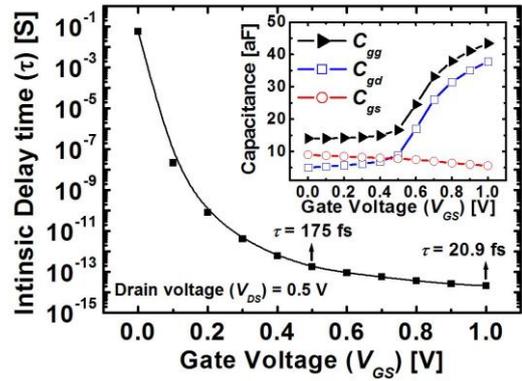


Fig. 4 Switching performance of $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ heterojunction TFETs as a function of V_{GS} ($V_{DS} = 0.5 \text{ V}$).

supply voltage, which is V_{DS} in this work, gate capacitance (C_{gg}) is the sum of intrinsic gate-to-drain capacitance (C_{gd}) and gate-to-source capacitance (C_{gs}), and I_{on} is I_D at a given V_{DD} . $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ heterojunction TFET shows significantly short τ above $V_{GS} = 0.5 \text{ V}$ owing to the higher I_{on} as well as small C_{gg} . TFET has genuinely small C_{gg} since it is affected by mainly C_{gd} as shown in the inset of Fig. 4, unlike conventional MOSFETs where both C_{gd} and C_{gs} are comparably contributing factors [7].

3. Conclusions

A tunneling field-effect transistor based on AlGaAs/InGaAs heterojunction has been studied and evaluated for LSTP and HP applications. The large difference between electron affinities of materials is proven to have a practical effect of narrowing the effective tunneling barrier width. The $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ heterojunction TFET demonstrated superb performances including I_{on} of $1.04 \text{ mA}/\mu\text{m}$, S of $22.6 \text{ mV}/\text{dec}$, and τ of 20.9 fs by the help of band engineering.

Acknowledgements

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References

- [1] G. Zhou, Y. Lu, R. Li, Q. Zhang, Q. Liu, T. Vasen, H. Zhu, J.-M. Kuo, T. Kosel, M. Wistey, P. Fay, A. Seabaugh, and H. Xing, IEEE Electron Device Lett. **33** (2012) 782.
- [2] S. Cho, I. M. Kang, T. I. Kamins, and B.-G. Park, and J. S. Harris, Jr., Appl. Phys. Lett. **99** (2011) 243505.
- [3] E.-H. Toh, G. H. Wang, G. Samudra, and Y.-C. Yeo, J. Appl. Phys. **103** (2008) 104504.
- [4] L. F. Register, M. M. Hasan, and S. K. Banerjee, IEEE Electron Device Lett. **32** (2011) 743.
- [5] Atlas User's Manual, Silvaco Inc. Santa Clara (2012).
- [6] A. Vandooren, D. Leonelli, R. Rooyackers, A. Hikavy, K. Devriendt, M. Demand, R. Loo, G. Groseneken, C. Huyghebaert, Solid-State Electron. **51** (2007) 572.
- [7] S. Cho, J. S. Lee, K. R. Kim, B.-G. Park, J. S. Harris, Jr., and I. M. Kang, IEEE Trans. Electron Devices **58**, (2011) 4164.