High-performance Single/Dual-layer Channel IGZO TFT Fabricated on Glass Substrates at Low-temperature

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Abstract

Fully-transparent amorphous indium gallium zinc oxide thin film transistors (a-IGZO TFTs) are fabricated on glass substrates at low temperature. Dual-layer channel IGZO TFTs are studied by changing partial pressure of oxygen in the sputtering chamber for comparison with single-layer ones which are fabricated without oxygen content changing. These low-temperature fabricated IGZO TFTs with dual-layer channel exhibit better performance than those with singer-layer channel. TFTs, of which the proportion of thicknesses of the two layers, low-oxygen layer and high-oxygen layer, is 3:1, demonstrate the best transfer characteristics with high on-to-off current ratio (I_{on/off}) of 1.8×10⁸. And TFTs of which the proportion of the thicknesses of two channel layers is 1:1 have highest on-current of 1.55mA and highest field effect mobility of 83.9cm²/V·s, and high $I_{on/off}$ ratio of 1.11×10⁸.

1. Introduction

Amorphous IGZO TFTs seem to be the most promising display devices, for its high mobility and good uniformity almost satisfy every requirement for OLED and large area and fast LCDs. These TFTs have high mobility of >10 cm²/V·s, typically small subthreshold swing (SS) in the range of 200~500mV/decade, and Ion/off ratio of about 10^4 to 10^9 [1][2]. Reports has been given intending to optimize electric characteristics of IGZO TFTs in different ways, for example, using high-k dielectric such as ZrO₂[3], and HfO₂[4], or using dual-gate structure [5], but they will either increase the cost of material or make fabrication more complicated. Characteristics of dual-layer channel has been studied in solution processing AIZO/IZO TFTs [6] and reactive sputtering ZnO TFTs [7], and the results show that dual-layer channel TFTs will have better performance if the resistance of the two layers and channel structure can be properly controlled. Works including that of ourselves have proven that the content of oxygen in the sputtering chamber while depositing IGZO will affect the resistance and thus affect the performance of the TFTs [8][9]. So in this work, we fabricate dual-layer channel TFTs by changing partial pressure of O₂ in the chamber, and study the electric characteristics of them.

2. Structure and Fabrication

These a-IGZO TFTs were fabricated using a bottom gate top contact structure as is shown in Fig. 1. Gate and source/drain electrodes whose thickness are about 150nm were deposited by rf sputtering at room temperature in Ar atmosphere using a target of ITO (Indium-Tin Oxide). Between them are 150nm thick gate insulator of SiO₂ formed by PECVD and an active layer of a-IGZO that is about 50nm thick formed by rf sputtering in Ar/O₂ atmosphere. IGZO layers were sputtered with different content of O₂ for different time as is shown in Table I, and thus the IGZO channel formed into single or dual layer channel as required. The dual-layer channel is composed of low-oxygen layer and high-oxygen layer. Because, as we know, the main carrier in ZnO-based thin film is oxygen vacancy [8], it makes low-oxygen layer high-resistance, and vice versa. The highest process temperature is 80 centigrade in the PECVD process, other layers using sputtering are deposited at room temperature. These layers were all patterned by standard photolithography and lift-off techniques, only the gate insulator and the active layer shared one photo mask in order to simplify the process of TFTs and optimize the interface between active channel layer and dielectric layer.



Fig. 1 (a) Cross-sectional schematic view of dual-layer channel TFT structure. (b) Photo of TFT top figure taken by microscope.

3. Results and Discussion

The TFTs were electrically characterized at room temperature by a semiconductor parameter analyzer (Agilent 4156C). Fig.2 show transfer curves of TFTs with single-layer channel and different structure of dual-layer channel. The width-to-length ratio of samples we tested is about 100μ m/10 μ m. The curves are got at V_{DS}=5V,



Fig. 2 These curves are of three types of TFTs with different structure of channel layer. From up to bottom are single low-oxygen layer (T1), dual-layers that the proportions of the layers are 3:1 (T2) and 1:1 (T3), respectively.

Because main carrier in ZnO-based thin film is oxygen vacancy, when oxygen content increases in the sputtering chamber, the IGZO thin film will have lower resistance, and we put this low-resistance layer further to the S/D contact. So According to our speculation, when V_G is very small, the high-resistance layer will play a major role of conducting layer; while V_G increases, the low-resistance layer will take the place of current transmission. Thus these TFTs will have larger I_{on} and not-so-large I_{off} .

These TFTs, as we can see, all show high $I_{on/off}$ of larger than 10⁷. And they also have very low subthreshold swing (SS) all lower than 0.2V/decade. But compared to T1, the single-layer channel TFTs, T2 and T3 both have larger on-current, and relatively lower off-current, that makes $I_{on/off}$ ratio of T2 and T3 became larger to about 10⁸, and performs better than the single-layer TFTs. Besides, T2 and T3 has very high mobility of larger than $60 \text{cm}^2/\text{V} \cdot \text{s}$. It means that T2 and T3 have indeed formed dual-layer channel structure, and perform better.



Fig. 3 Output curves of T1 measured at different V_G in the range of 0V~3V, by step of 0.5V.

Output curves shown in Fig. 3 illustrate that the contact between S/D electrode and active layer is good. Though crowding effect still exist, it doesn't affect the saturation state very much. By the way, saturation current exceeded $40\mu A$ at a relatively a low V_G, it's also an evidence of its high mobility and good performance.

Data extracted from these curves are listed in Table I in order to compare the characteristics of T1, T2 and T3. Since when the thickness of low-oxygen layer increases, I_{on} became larger and mobility higher, thicknesses of the two layers will also affect the TFTs' performance.

Table I Electrical Parameters of Single/Dual-layer TFTs

TT1 T		
11 1	2 T3	
.05Pa	0.01Pa&0.05Pa	
20min 5min/1	5min 10min/10)min
0.37 0.9	00 1.55	
24 5	14	
54×10^7 1.8×	10 ⁸ 1.11×1	0^{8}
178 17	3 174	
38.6 70	.7 83.9	
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4. Conclusions

We studied dual-layer channel effect on electrical properties of the IGZO TFTs. The results showed that we can control the resistance of IGZO thin film by changing the oxygen content in the sputtering chamber, thereby we can build dual-layer channel device in that way. And if we choose proper structure of dual-layer channel and control the two layers' resistance, the dual-layer channel TFTs will have better performance than the single layer ones.

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References

- T. Kamiya, K. Nomura, and H. Hosono, Science and Technology of Advanced Materials. 11.4 (2010) 044305.
- [2] K. Nomura., H. Ohta., A. Takagi, et al., Nature. 432.7016 (2004) 488.
- [3] J. S. Lee, S. Chang, S. M. Koo, *et al.*, IEEE Electron Device Letters. 31.3 (2010). 225.
- [4] Liang-Yu Su, Hsin-Ying Lin, and Huang-Kai Lin, et al., IEEE Electron Device Letters. 32.9 (2010) 1245.
- [5] Gwanghyeon Baek, Katsumi Abe, and Alex Kuo, *et al.*, IEEE Transaction n Electron Devices. 58.12 (2011) 4344.
- [6] Kyung Min Kim, Hee Jeong, and Dong Lim Kim, *et al.*, IEEE Electron Device Letters. **32.9** (2011) 1242.
- [7] Shao-Juan Li, Xin He, De-Dong Han, and Yi Wang, et al., Solid-State and Integrated Circuit Technology (2012).
- [8] Jianke Yao, Ningsheng Xu, and Shaozhi Deng, et al., IEEE Transaction on Electron Devices. 58.4 (2011) 1121.
- [9] Yu Tian, Dedong Han, and Yi Wang, et al., Electron Devices and Solid State Circuit (2012).