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Improved Stability of ZnO Thin Film Transistor with Dual Gate Structure under Negative Bias Stress

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Abstract

In this paper, we have fabricated the dual-gate zinc oxide thin-film-transistors (ZnO TFTs) without additional process and post treatment and analyzed the stability characteristics under the negative bias stress (NBS) comparing with the conventional bottom gate structures. The dual gate device shows the superior electrical parameters such as subthreshold swing (SS), on/off current ratios. NBS of V_{GS}= -20 V with V_{DS}=0 was applied and negative threshold voltage (V_{th}) shift was observed. After 10^3 sec stress applied, V_{th} shift is 0.60 V in dual gate structure while V_{th} shift is 2.52 V in bottom gate ZnO TFT. As the simulation shows, this stress immunity of the dual gate structure is caused by the change of field distribution in the ZnO channel by adding another gate.

1. Introduction

Organic light-emitting diode (OLED) and AMLCD devices are the major constituents of flat panel display products that generally use amorphous Si (a-Si) thin film transistor (TFT) as gate driver and pixel switching devices [1]. But, a-Si TFT has some drawbacks, such as low mobility, light sensitivity and opacity. Zinc oxide (ZnO) semiconductors have been extensively studied with much attention as an active channel material because they offer high performance, low temperature process and transparency. But, it is well known that ZnO TFT has an instability problem under the gate bias [2] - [3]. Considering that the switching TFT of AMOLED display is most of the time experiencing a negative gate bias in its off state [4], it is necessary to improve the instability of ZnO TFT under negative bias stress (NBS). In this paper, in order to improve stability of ZnO TFT, we have fabricated the ZnO TFT with dual gate structure and analyzed the electrical chracteristic with NBS comparing with the conventional bottom gate structures.

2. Experiment

Figure 1 is the schematic cross section of the fabricated dual-gate ZnO TFTs with 200-nm-thick SiNx for both top and bottom dielectrics. The fabrication process was as follows, a 100-nm-thick Ti was deposited as a bottom gate by RF magnetron sputtering and patterned by lithography and dry etch process. Then, a 200-nm-thick SiNx was deposited as the gate insulator by conventional PE-CVD at 400 °C and 100-nm-thick Ti was deposited as a channel pad by RF magnetron sputtering and patterned by lithography and dry etch process. The ZnO channel layers with 100-nm-thick was deposited on the gate insulator and channel pad by using a RF magnetron sputtering in Ar/O2 (60%/40%) at 100 °C . A 50-nm-thick SiNx film was deposited on the ZnO by PE-CVD at 150 °C in order to protect the body of ZnO TFT. The SiNx and ZnO films were patterned by the dry etching. The dry etching gases of ZnO were HBr and Ar. After definition of the active channel, a 150-nm-thick SiNx for interlayer dielectric was deposited by PE-CVD at 150 °C. Contact holes for source and drain electrodes were opened by the dry etching. And then a 100-nm-thick Ti for source/drain electrodes and a top gate was deposited by RF magnetron sputtering at 200 °C and was patterned by the dry etching. The channel length and width are 8 μm and 40 μm, respectively. For the comparison, the conventional bottom-gate TFT was also fabricated. The electrical characteristics were measured by a semiconductor parameter analyzer (HP4156C) and simulation is performed using Sentaurus devices 2D.

3. Result and Discussion

Figure 2 shows I_{DS}-V_{DS} characteristics of the fabricated conventional bottom gate and the dual gate ZnO TFT. It is seen that the ohmic contacts are well formed at the Ti/ZnO interface. In case of the dual gate device, the saturation appears more clearly than in the conventional bottom gate at high drain biases, which indicates that the channel of dual gate device is operating at the fully depletion mode [5]. Figure 3 shows I_{DS}-V_{GS} characteristics at a drain voltage = 12 V. The turn-on voltage appears -13.5V at the bottom-gate and -3V at the dual-gate, respectively. This positive shift of turn-on voltage shift in the dual gate device can be explained by the suppression of sub-channel in bottom gate device [6]. As for the field effect mobility, it is 0.88 $cm^2/V{\cdot}s$ in the conventional bottom gate while in the dual gate structure, the mobility is 0.45 $cm^2/V{\cdot}s$. The extracted mobility is lower than the bottom gate device, but in the dual gate device, electrical characteristics including the subthreshold swing (SS) and on/off current ratio are improved. In case of SS in the dual-gate is dramatically improved as 0.6V/decade, compared with conventional bottom-gate of 1.6V/decade. Other electrical characteristics including on/off current ratio and capacitance extracted parameters are given in table 1. To compare the electrical stability under NBS, the gate bias of -20 V is forced with a drain voltage = 0.1V. Figure 4 shows I_{DS}-V_{GS} characteristics after the negative gate bias stress. The inset of Fig. 4 (b) shows SS according to the stress time. SS is almost same throughout the stressing times both in the bottom gate and the dual gate device, which indicates the trap generation is ignorable under the stress condition. In case of turn-on voltage, however, the bottom gate structure exhib-

ited a large negative shift (2.52 V) with increasing stress time. In contrast, dual gate structure shifts only 0.6 V. Generally, the negative shift of turn-on voltage under the negative gate bias has been explained by the hole trapping via pre-existing traps. That is, after free holes are attracted to and accumulated at the active/dielectric interface following applied negative voltage, some of them would remain trapped at the interfacial states or penetrate into the gate dielectric layer resulting in the negative shift of transfer curve as the stress time increases [3]. In case of dual gate structure, it is possible that when the gate bias is applied at both side of channel, there is the electric field cancellation phenomenon. To verify this hypothesis, the electric field distribution of ZnO channels is analyzed using TCAD simulation. Figure 4 shows the simulation results of electric field distribution in bottom and dual gate ZnO device. In the case of bottom gate structure, by the applied voltage of bottom gate, electric field is formed primarily at the bottom of the ZnO layer. On the contrary, in case of dual gate structure, the electric field is weaker than the bottom gate due to the interference of electric field of the top side and bottom side. Figure 4-(c) shows relative amount of electric field in ZnO layer as function of gate structure. This cancellation effect have resulted much smaller negative shift under NBS.

4. Conclusions

The device stability and performance of ZnO TFTs are dramatically improved using dual gate structure without additional process and post treatment. The fabricated dual gate device has superior electrical properties. When the gate bias is applied at both side of channel in dual gate structure, the interference of electric field of the top side and bottom side has the cancellation effect on the active layer causing much smaller negative shift under NBS.

Acknowledgements

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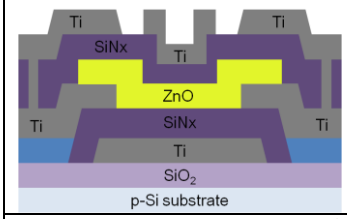
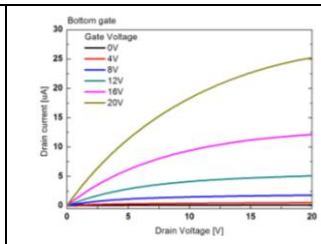
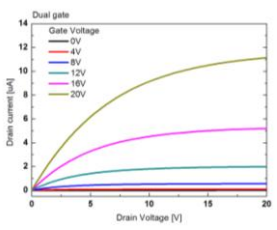


Fig. 1. Schematic cross section of the ZnO TFT with dual gate structure. Channel length (L): 5um, channel width: 40um.



(a)



(b)

Fig. 2. Output characteristics of the ZnO TFTs as function of: (a) conventional bottom gate, (b) dual gate structure.

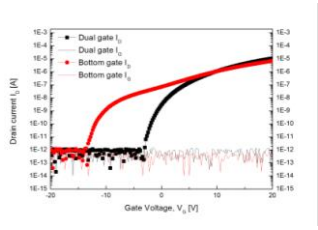
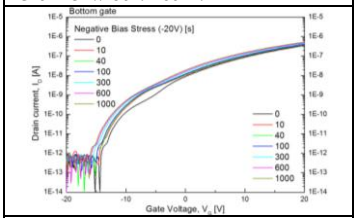
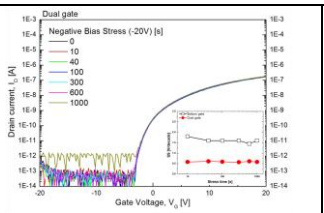


Fig. 3. Transfer characteristics of the ZnO TFTs at a drain voltage = 12 V as function of conventional bottom gate and dual gate structure.



(a)

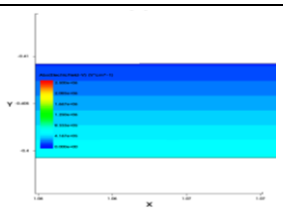


(b)

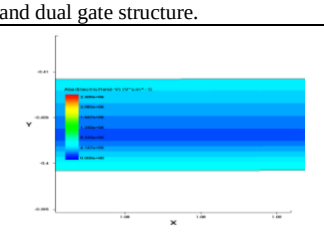
Fig. 4 Transfer characteristics of the ZnO TFTs at a drain voltage = 0.1V with gate bias stress of -20 V as function of: (a) conventional bottom gate, (b) dual gate structure, and change in subthreshold slope with stress voltage for different stress times(inset).

Table 1. Electrical characteristic of ZnO TFT as function of gate structure

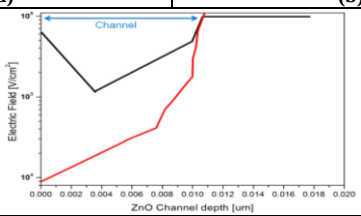
Structure	V_{th} [V]	SS [V/decade]	On/Off current ratio	Mobility [$cm^2/V•s$]	Capacitance [nF/cm^2]
Bottom gate	-10.75	1.6	9.16 x 10^6	0.88	31.9
Dual gate	-0.45	0.6	1.46 x 10^7	0.49	54.9



(a)



(b)



(c)

Fig. 5 TCAD simulation results of the electric field distributions in ZnO channel as function of: (a) bottom gate, (b) dual gate.