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Effects of High-Temperature Annealing on Properties of Al_2O_3/InAlN Interface Formed by Atomic Layer Deposition

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Abstract

Effects of high-temperature annealing on the properties of the Al_2O_3/InAlN interface formed by atomic layer deposition (ALD) are investigated. Post deposition annealing at 850 °C deteriorated the electrical property of the InAlN metal-oxide-semiconductor diode with an 18 nm-thick ALD-Al_2O_3 layer. However, the Al_2O_3/InAlN interface property was improved by two-step ALD interrupted by annealing at 850 °C right after the initial 2 nm-thick Al_2O_3 layer formation.

1. Introduction

InAlN lattice matched to GaN is one of the candidate barrier materials for high frequency and high power GaN-based high-mobility-electron transistors (HEMTs) [1]. For a high performance of HEMTs, use of a gate insulator to suppress the leakage current has been proposed [2]. Recently, a marked progress of the cut-off frequency of InAlN/GaN HEMTs has been achieved by inserting a gate insulator [3]. However, a control method of the insulator/InAlN interfaces, particularly annealing to improve the interface properties, has not been matured. Although Al_2O_3 by atomic layer deposition (ALD) is promising for a gate insulator, it should be taken into account that annealing at a high temperature causes crystallization of Al_2O_3 to deteriorate insulating properties [4]. Here, actual effects of high temperature annealing on the ALD-Al_2O_3/InAlN interface properties are investigated to find an appropriate method.

2. Sample preparation

Here, a fabrication process for a metal-oxide- semiconductor (MOS) diode illustrated in Fig. 1 is adopted in order to separate the annealing effects on the Al_2O_3/InAlN interface from those on the Al_2O_3 bulk. The process sequence is as follows. Tested MOS diodes consisted of the ALD-Al_2O_3 (18 nm)/n-$In_{0.17}Al_{0.83}N$ (160 nm, $n = 2\times10^{18}$ cm^{-3}) structures. An annular Ti/Al/Ti/Au (20 nm/50 nm/20 nm/100 nm) ohmic contact was formed and annealed at 850 °C for 1 min using a 20 nm-thick SiN_x cap layer for surface protection. After removing the SiN_x cap layer using buffered hydrofluoric acid, a 2 nm-thick ALD-Al_2O_3 layer was formed at 350°C using H_2O and trimethylaluminum. Subsequently, the sample was annealed at 850°C for 1 min. Then, the outer Al_2O_3 layer of 16 nm thickness was deposited by ALD again. Finally, a circular Ni/Au (20 nm/50 nm) electrode was formed on the Al_2O_3 layer at the center of the annular ohmic electrode. For comparison, MOS diodes with an Al_2O_3 layer of 18 nm thickness by conventional one-step ALD without interruption were also prepared. Post deposition annealing for these was performed prior to Ni/Au electrode formation. For XPS investigation, a 15 nm-thick InAlN layer on the GaN buffer layer was used.

3. Results and discussion

The 1 MHz capacitance-voltage (C-V) curves measured before and after post deposition annealing at 850°C for 1 min are compared in Fig. 2 for the MOS diodes fabricated by one-step ALD without interruption. After annealing the C-V characteristic was markedly deteriorated compared with that of the as-deposited sample, which indicated that post deposition annealing at a high temperature was not suitable for this structure.

In order to investigate the influence of annealing on the interface, X-ray photoelectron spectroscopy (XPS) investigation was performed on the sample with 2 nm-thick Al_2O_3 layer on InAlN. The In 4d spectra measured before and after annealing at 850 °C for 1 min are shown in Fig. 3. There was no marked evidence of intermixing at the interface. This result indicates that high-temperature annealing does not necessarily deteriorate the interface structure.

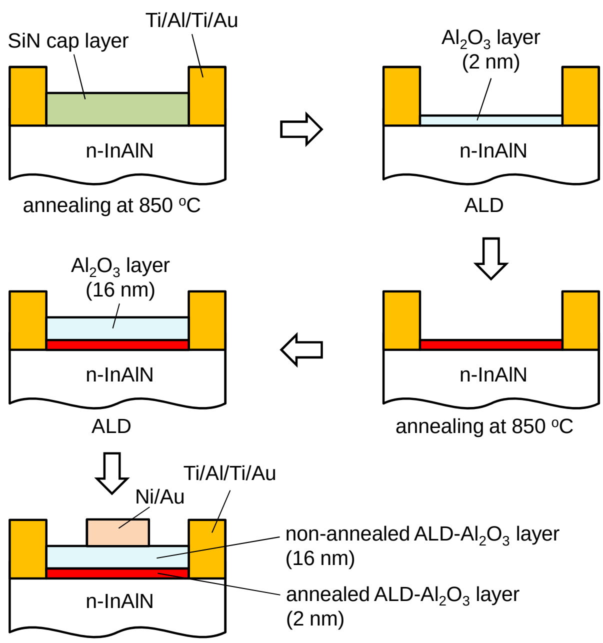

Fig 1 Fabrication process with two-step ALD.

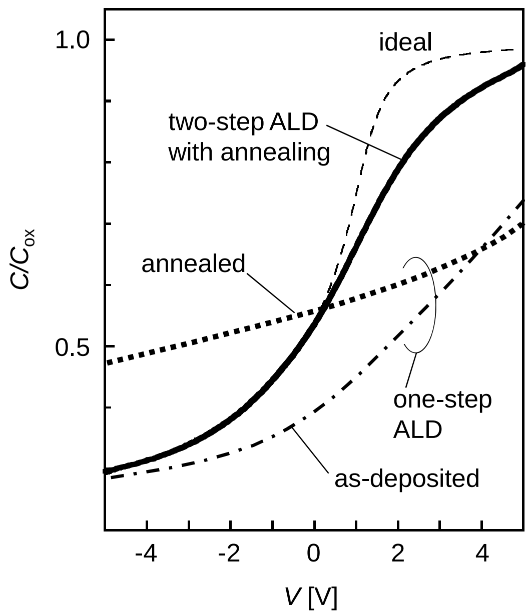

Fig 2 C-V curves. The solid line indicates the 1 MHz curve for the MOS diode through two-step ALD combined with annealing, while the one-dot-chain and dotted lines are respectively those for the one-step ALD samples before and after annealing at 850 °C. The broken line shows the ideal curve.

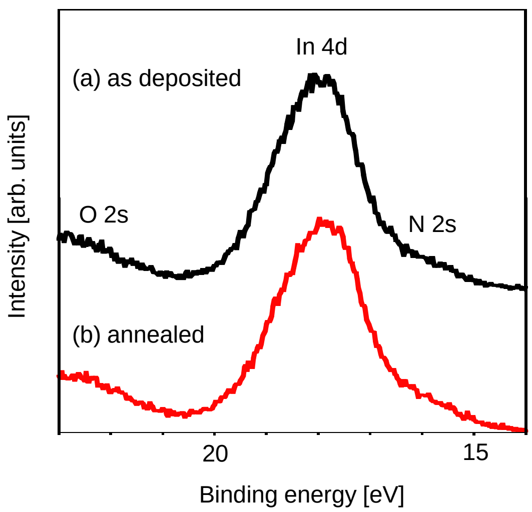

Fig 3 XPS In 4d spectra with N 2s and O 2s spectra of the Al_2O_3(2 nm)/InAlN sample measured (a) before and (b) after annealing at 850 °C for 1 min.

There is the possibility that the deterioration of the electrical properties of the MOS diode was owing to the bulk of the Al_2O_3 layer. Therefore, we tried to apply the proposed interface formation method. Actually, the C-V curve measured for the two-step ALD sample showed a much improved characteristic with a large capacitance change, as shown in Fig. 2 where the ideal curve overlaps the measured one in the depletion region. This result indicates that the reduction of the interface states while maintaining the high dielectric quality was achieved by adopting

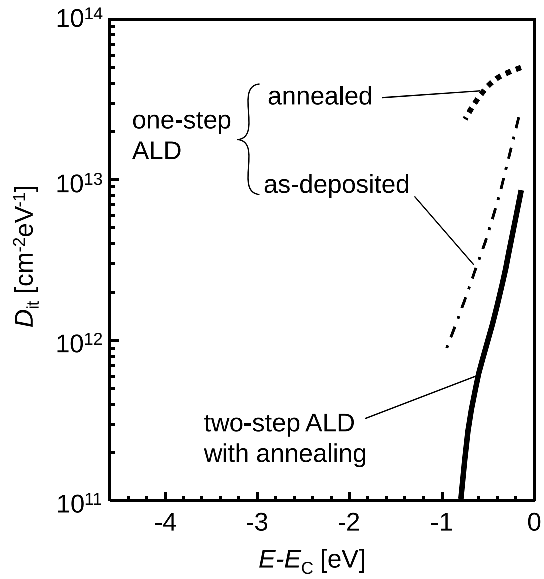

Fig 4 D_{it} distributions evaluated from C-V curves.

the two-step ALD method.

The D_{it} distribution was evaluated for all samples by the high-frequency method, as shown in Fig. 4. The D_{it} evaluation is limited to near the conduction band because the time constant of the interface states becomes much longer than the practical measurement time deep inside the band gap. Although high-temperature annealing led to an increase in D_{it} for the sample through one-step ALD, D_{it} was markedly reduced for the two-step ALD sample. Therefore, the interface properties are improved by high-temperature annealing when the deterioration of the Al_2O_3 insulator bulk properties, probably owing to crystallization [4], is suppressed.

4. Conclusions

Although the electrical properties of the MOS diode with the single ALD-Al_2O_3 layer was deteriorated, XPS results showed that annealing at 850 °C was not harmful for the ALD-Al_2O_3/InAlN interface. Thus, the deterioration of the diode properties was possibly caused by the annealed Al_2O_3 insulator bulk. Actually, an improvement of the Al_2O_3/InAlN interface properties was achieved by minimizing annealed layer thickness in two-step ALD.

Acknowledgements

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