GaSb-on-insulator metal-oxide-semiconductor field-effect transistors on Si fabricated by direct wafer bonding technology

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Abstract

We have developed a wafer-scale GaSb-on-insulator (GaSb-OI) on a Si wafer by direct wafer bonding (DWB) technology and have demonstrated p-type GaSb-OI metal-oxide-semiconductor field-effect transistors (pMOSFETs) on a Si wafer. The GaSb-OI structure on Si shows the Hall mobility of ~300 cm²/Vs with carrier density (Nᵥ) of ~3.1×10¹⁷ cm⁻³. A GaSb-OI pMOSFET under accumulation-mode operation exhibits a peak effective mobility of ~79 and ~181 cm²/Vs at 295 and 7 K, respectively, at a surface charge density (Nₛ) of ~5.5×10¹⁵ cm⁻².

1. Introduction

III-V compound semiconductor channel MOSFET devices can be a candidate promising for CMOS devices in post-scaling generation [1]-[6]. Sb-based III-V compounds are promising channel materials for pMOSFET devices because of their high hole mobility [7]-[10]. One of the critical issues for realizing Sb-based MOSFETs on CMOS platform is the integration of III-Sb channels with Si wafers, because the large lattice mismatch between III-Sb and Si can cause the difficulty in the direct growth on Si. Recently, the transfer of In₃₋₅GaₓSb nanoribbons on Si substrates has been demonstrated by epitaxial lift-off technique with polydimethylsiloxane (PDMS) [10]. However, it is difficult to employ the wafer-scale transfer of III-Sb layers and this transfer technique using PDMS can generate dislocations in the transferring channel during transfer process. Thus, we have newly developed a process of wafer-scale transfer of III-V layers on Si wafers with retaining excellent crystal quality using DBW technology [3]-[5]. We have reported [5] that DBW can realize transfer high crystal quality InGaAs layers even with the extremely thin channel thickness of 3 nm. In this paper, we report the wafer-scale GaSb-OI layer transfer on Si by DBW technology and demonstrate the operation of GaSb-OI pMOSFETs on Si.

2. Fabrication of GaSb-OI on Si wafer by DBW

We have fabricated GaSb-OI-on-Si wafers by DBW with Al₂O₃ buried oxide (BOX) layers [4],[5]. Figure 1(a) shows the fabrication process flow of GaSb-OI on Si wafers. Firstly, 50-nm-thick GaSb layers were grown on 2-inch (100) InAs wafers. Figure 1(b) shows an atomic-force microscope (AFM) image of an as-grown GaSb/InAs surface. The Rₘₐₓ value is as small as ~0.17 nm, which is enough to perform direct wafer bonding [3]-[5]. Then, Al₂O₃ BOX layers were deposited on both GaSb/InAs and Si wafers by atomic-layer deposition (ALD). Figure 2(a) shows the capacitor versus voltage (C – V) curves measured at the frequency of 1 MHz of the Al₂O₃/p-GaSb MOS capacitors fabricated at several ALD temperature (T_AlD) with pre-cleaning by an HCl solution. The carrier concentration (Nᵥ) of p-type GaSb was 1.85×10¹⁶ cm⁻³. The red, blue, green, and black colored curves are for C – V curves fabricated at T_AlD of 150, 200, 250, and 300 °C, respectively. The solid and broken curves correspond to the measurements by sweeping the voltage from accumulation voltage (V_acc) to inversion voltage (V_inv) and from V_inv to V_acc, respectively. We have found that the GaSb MOS capacitors have the strong T_AlD dependence and that the GaSb MOS interface fabricated at the T_AlD of 150 °C is better than the others. As a result, we have deposited the ALD Al₂O₃ layer on the GaSb/InAs wafer at T_AlD of 150 °C. Subsequently, the wafers were manually bonded in air. After bonding the wafers, the InAs substrates were etching by H₃SO₄:H₂O₂ and citric acid peroxyde solutions. The InAs wafer was etched down to ~100 µm using an H₂SO₄:H₂O₂ solution. The rest of InAs was selectively etched using citric acid peroxyde solution and the GaSb-OI on Si wafer completed.

Figures 3(a) and 3(b) shows cross-sectional transmission electron microscope (TEM) images of the GaSb-OI on Si wafer and GaSb/Al₂O₃ and Al₂O₃/InAs interfaces. Figure 3(c) shows the XRD spectrum from the GaSb-OI-on-Si wafer, indicating the transferred GaSb retains an excellent crystal quality. The ALD Al₂O₃ BOX DWB process can show the good compatibility for fabrication GaSb-OI on Si wafers.

\[ \text{Fig. 1 (a) Fabrication process flow of GaSb-OI on Si wafers by DWB technology. (b) AFM image of an as-grown 50-nm-thick GaSb layer on a (100)-oriented InAs wafer.} \]

\[ \text{Fig. 2 } C - V \text{ curves measured at the frequency of 1 MHz of the Al₂O₃/p-GaSb MOS capacitors fabricated at T_AlD of 150, 200, 250, and 300 °C, respectively.} \]
3. GaSb-OI pMOSFETs on Si wafer

We have fabricated GaSb-OI pMOSFETs on Si with back-gate configuration. Figure 4(a) shows the fabrication process flow of GaSb-OI pMOSFETs on a Si wafer with back-gate configuration. The GaSb-OI layer was isolated by wet-etching using a H₃PO₄:H₂O₂:H₂O (= 1:1:7) solution at room temperature for ~ 30 sec. Then, Ni (~ 60 nm) and Al (~ 240 nm) was deposited on the GaSb-OI channels by a thermal evaporator as S/D contacts. Finally, Al (~ 200 nm) was deposited on the Si wafer by a thermal evaporator as a back-gate contact. Here, a phosphorous doped n-Si wafer with 0.001 ~ 0.0015 ρcm was used as a bonded Si wafer and as a back gate. Figure 4(b) shows an AFM image of the GaSb-OI surface after removing the InAs wafer. The $R_{\text{int}}$ value is as small as ~ 0.92 nm. We evaluated the bulk properties of the GaSb-OI layer by Hall effect measurements. The GaSb-OI layer was p-type and $\mu_{\text{Hall}}$ and $N_D$ of the GaSb-OI layer are estimated to be ~ 300 cm²/Vs and ~ 3.1×10¹⁶ cm⁻³, respectively. This result means that the fabricated GaSb-OI pMOSFETs operate under accumulation mode. Figures 5(a) and 5(b) show the drain current versus drain voltage ($I_D - V_D$) and the effective hole mobility versus surface carrier density ($\mu_{\text{eff}} - N_s$) curves, respectively, of the fabricated GaSb-OI pMOSFETs on a Si wafer with gate length ($L_g$) of 500 μm. The red, blue and black colored curves show for the curves measured at 7, 100, and 295 K, respectively. A black square symbols in Fig. 5(b) also shows the $\mu_{\text{eff}} - N_s$ curve of Si pMOSFETs with substrate concentration ($N_{\text{sub}}$) of 3.1×10¹⁷ cm⁻³. As shown in Figs. 5(a) and 5(b), the transistor operation was confirmed. However, the on-off current ratio was not good even at low temperature. As shown in Fig. 5(b), the peak effective mobility was ~ 79 cm²/Vs at $N_s$ of ~ 5.5×10¹² cm⁻² at 295 K. The peak effective mobility at 7 K was ~ 187 cm²/Vs. The $\mu_{\text{Hall}}$ Values of the present GaSb-OI pMOSFETs are comparable to the Si pMOSFETs. However, this peak $\mu_{\text{Hall}}$ value of ~ 70 cm²/Vs is much lower than the fairly high $\mu_{\text{Hall}}$ value of ~ 300 cm²/Vs in spite of the fact that the fabricated transistors operate under accumulation mode, which can reflect the bulk mobility. Since the Ni/p-type GaSb junctions can exhibit ohmic contacts [11] and the long channel devices are used for mobility evaluation, the impact of the S/D resistance on the mobility extraction can be regarded as negligible. On the other hand, as shown in Fig. 2, the Al₂O₃/GaSb MOS interface properties are known to be still poor because of the large interface trap density of ~ 10¹³ ~ 10¹⁴ eV·cm⁻² [12], though the interface would be better than the GaSb MOS gate stacks with the other gate insulators. As a result, the observed low $\mu_{\text{Hall}}$ values are attributable to the inferior GaSb MOS interface properties. We have also found high off-current as shown in Fig. 5(a), and the high off-current also explained by this weakly-pinched surface potential due to large interface state density. Thus, improvement of the GaSb-OI MOS interface property can be a key to achieve the high performance GaSb-OI pMOSFETs on Si wafers.