Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp148-149

A Device Performance Study of Stacked Gate Dielectrics AlGaN/GaN MOS-HEMTs by Mixed Oxide Thin Film Growth Techniques

Bo-Yi Chou, Yu-Sheng Wu, E-Ling Huang, Wei-Fan Chen, Han-Yin Liu, Wei-Chou Hsu*, Ching-Sung Lee[1], Wen-Chia Ou, and Chiu-Sheng Ho
Institute of Microelectronics, Department of Electrical Engineering, and Advanced optoelectronic Technology Center, National Cheng Kung University, Tainan 70101, Taiwan
Phone: +886-6-2757575#62350; E-mail: wchsu@eembox.ncku.edu.tw
[1]Department of Electronic Engineering, Feng Chia University, Taichung 40724, Taiwan

Abstract

This paper reports an AlGaN/GaN metal-oxide-semiconductor high electron mobility transistor (MOS-HEMT) with stacked Al_2O_3/HfO_2 gate dielectrics by using hydrogen peroxide (H_2O_2) oxidation/sputtering techniques. The present Al_2O_3/HfO_2 bi-layer MOS-HEMTs can combine the advantages of both gate dielectrics and have demonstrated enhanced drive current, breakdown, and power characteristics.

***Index Terms*- MOS-HEMT, Al_2O_3/HfO_2, high-k, H_2O_2 oxidation, sputtering.**

1. Introduction

The AlGaN/GaN HEMTs have attracted much attention for high frequency and high power applications because of the GaN material shows wide band-gap, high breakdown field, and high electron saturation velocity [1]. But most of Schottky-gate HEMTs usually suffer from serious gate leakages [2]. Hence, many studies have been devoted to improving the gate insulating by MOS gate structures with high-k materials [3-6]. Recently, high-k materials like Al_2O_3 and HfO_2 have been widely studied due to them exhibit high dielectric constant, wide band-gap, and effectively used in decreased the gate leakages and power consumption. In the previous studies [6-7], we reported that Al_2O_3 passivation/gate dielectric is effectively suppressed the gate leakages, surface traps, and power dissipation. In order to improve device performance and equivalent oxide thickness (EOT), high-k dielectrics are beneficial for the above conditions. Therefore, in this work, the device performance of the present MOS-HEMT with Al_2O_3/HfO_2 stacked gate dielectrics design are investigated with respect to a Schottky-gate device.

2. Material growth and Device Fabrication

The studied device was grown by using a metal-organic chemical vapor deposition system. Upon a sapphire substrate, the device epi-layers consist of a 30-nm GaN nucleation layer, an undoped 2-μm GaN buffer layer, and an undoped 30-nm $Al_{0.27}Ga_{0.73}N$ barrier layer. Device fabrication started with the mesa etching and source/drain electrodes were formed by depositing Ti/Al/Ni/Au metal stacks. Drain-source ohmic contacts were formed by performing RTA at 900℃ for 60 seconds. For the stacked Al_2O_3/HfO_2 gate dielectrics MOS-HEMT (sample A), Al_2O_3 was formed first by performing H_2O_2 oxidization immersing into H_2O_2 solution for 5 minutes to perform the 8 nm Al_2O_3 film. Then, the 5 nm HfO_2 dielectric was directly deposited upon the Al_2O_3 film by sputtering. Finally, Ni/Au metal stacks were deposited and lift-off to define the gate electrode. A Schottky-gate device (sample B) was fabricated on the same epitaxial structure, except without performing the gate dielectrics process. The gate dimensions for the studied devices are 1×100 μm^2 with a source-to-drain spacing of 7 μm. From C-V measurement, relative permittivity (k) of sample A was determined to be 11.5 and EOT values of sample A were decreased from 5.5 nm to 4.4 nm as compared to the MOS-HEMT with Al_2O_3 dielectric only [6].

3. Results and Discussion

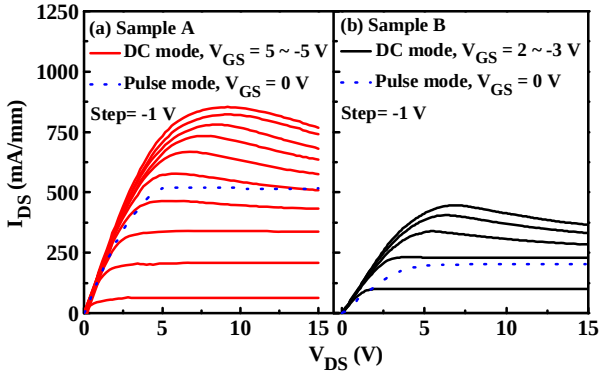

Fig. 1 DC- and pulse-mode I_{DS}–V_{DS} characteristics of samples (a) A and (b) B.

The DC characteristics of both devices were measured by Keithley 4200 system. Figures 1(a)-(b) show the common-source current-voltage (I_{DS}-V_{DS}) characteristics of samples A and B. The maximum drain-source current density ($I_{DS,\ max}$) and saturation drain current density at V_{GS}= 0 V (I_{DSS0}) were determined to be 830.6/471 mA/mm and 582.4/334.7 mA/mm for samples A/B. The sample A exhibits the larger $I_{DS,max}$ and I_{DSS0} than sample B. This is attributed to further reduce the gate leakages and improve gate insulating performance by stacked gate dielectrics, which will be discussed later. On the other hand, RF current collapse is analyzed by pulse I–V measurement which is also compared in figs. 1(a)-(b). For fair comparison, the devices were biased at V_{GS} = 0 V. The pulse width is set to be 10 μs. Lower discrepancies at V_{DS} = 6 V in sample A than sample B was observed. Good surface passivation effects of the Al_2O_3/HfO_2 dielectrics have also been confirmed by the

pulsed I-V results. This clearly indicates that the surface traps in the drain-source region have been effectively annihilated after the H_2O_2 oxidation treatment.

Two-terminal gate–drain (I_{GD}–V_{GD}) characteristics of samples A/B are shown in fig. 2. The two-terminal gate-drain breakdown/turn on voltages (BV_{GD}/V_{ON}) are defined as the corresponding V_{GD} biases, where the I_{GD} magnitude is equal to 1 mA/mm. BV_{GD}/V_{ON} were found to be -146.5/2.11 V and -78/1 V for samples A and B. Furthermore, the gate leakage currents (I_{GD}) are 8.6×10^{-5} mA/mm and 5.6×10^{-1} mA/mm at V_{GD} = -30 V for samples A and B. Obviously, much lower I_{GD} is obtained in sample A than in sample B. The hot carriers in the channel layer overcome the Schottky barrier height by thermionic emission and thermionic field emission, both of which have degraded the I_{GD} characteristic in sample B. In addition, the three-terminal off-state breakdown voltage (BV_{off}) of samples A/B are 132/64 V at V_{GS} = -6 V as shown in the inset of fig. 2. The previous studies have discussed that BV_{off} mainly resulted from the impact ionization which occurred at the edge of gate electrode near the high-field region [8]. Gate leakage injection is the dominant source to trigger impact ionization mechanism at high V_{DS} bias [9]. The present MOS-HEMT with enhanced gate-insulating property effectively suppresses the gate leakage injection and consequently improves the BV_{off} characteristic as compared with sample B.

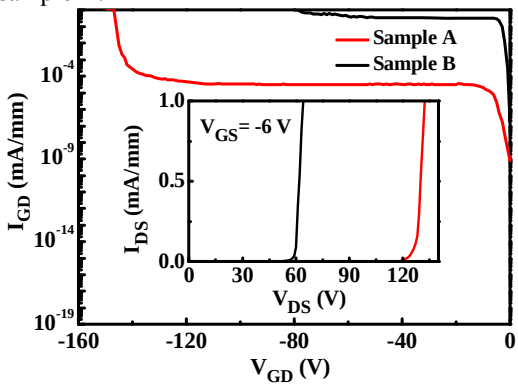

Fig. 2 Two-terminal I_{GD}–V_{GD} characteristics of samples A and B under reverse biases. The inset shows BV_{off} characteristics for studied devices.

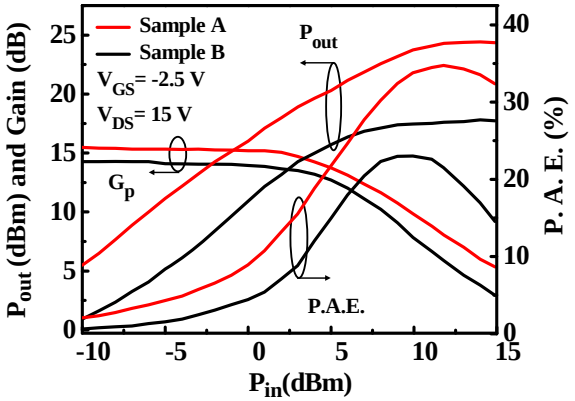

Fig. 3 P_{out}, G_p, and P.A.E. characteristics measured at 2.4 GHz for samples A and B.

Fig. 3 shows the output power (P_{out}), power gain (G_p), and power-added efficiency (P.A.E.) characteristics at 2.4 GHz for the studied devices, measured on-wafer by the load-pull system. Maximum P_{out}/G_p/P.A.E. for samples A and B were found to be 24.3 dBm/16.23 dB/34.7% and 18.02 dBm/14.27 dB/23.03% at V_{GS} = -2.5 V and V_{DS} = 15 V, respectively. P_{out} and P.A.E. can be expressed as P_{out}= $\{(BV_{GD}-V_{knee})\times I_{DS,\ max}\}/8$ and PAE = $\{(P_{out}-P_{in})/P_{DC}\}\times100\%$ [10], where V_{knee} is the knee voltage and P_{dc} is the dc power dissipation. Improved power performances of sample A are resulted from enhanced current drive, decreased P_{dc} dissipation, and suppressed gate leakage current because of the good passivation effect and gate insulating by the present stacked MOS-HEMT design.

3. Conclusion

In this report, we proposed an Al_2O_3/HfO_2 stacked gate dielectrics by using mixed oxide thin film techniques. Device performances are improved due to the present MOS-HEMT improved gate insulating and enhanced drive current capability by devising stacked gate dielectrics MOS-HEMT design. Consequently, the present MOS-HEMT design using the cost-effective H_2O_2 oxidation and high-k HfO_2 thin film that can further improve gate leakages, enhance drive current, and more suitable for high-power applications.

Acknowledgements

This work was supported in part by the National Science Council, Taiwan, under contract numbers of NSC 100-2221-E-006-039-MY3, NSC 100-2221-E-006-041- MY3, and NSC 102-2218-E-006-007-, and in part by Advanced Optoelectronic Technology Center of NCKU.

References

[1] M. Kameche and N.V. Drozdovski, Microwave J., **48** (2005) 164.

[2] L. H. Huang, S. H. Yeh, C. T. Lee, H. P. Tang, J. Bardwell, and J. B. Webb, IEEE Electron Device Lett., **29** (2008) 284.

[3] Y. Nakano, T. Kachi, and T. Jimbo, Appl. Phys. Lett., **83** (2003) 4336.

[4] S. Yang, S. Huang, H. W. Chen, C. H. Zhou, Q. Zhou, M. Schnee, Q. T. Zhao, J. Schubert, and K. J. Chen, IEEE Electron Device Lett., **33** (2012) 979.

[5] C. Liu, E. F. Chor, and L. S. Tan, Semicond. Sci. Technol., **22** (2007) 522.

[6] H. Y. Liu, B. Y. Chou, W. C. Hsu, C. S. Lee, and C. S. Ho, IEEE Electron Device Lett., **33** (2012) 997.

[7] H. Y. Liu, B. Y. Chou, W. C. Hsu, C. S. Lee, and C. S. Ho, IEEE Trans. Electron Devices, **58** (2011) 4430.

[8] Y. Ohno, T. Nakao, S. Kishimoto, K. Maezawa, and T. Mizutani, Appl. Phys. Lett., **84** (2004) 2184.

[9] H. Kim, J. Lee, D. Liu, and W. Lu, Appl. Phys. Lett., **86** (2005) 143505.

[10] F. Ren and J. C. Zolper, *Wide Energy Bandgap Electronic Devices*, (2003) 192.