Pn-Diode-Structured p-CuOₓ/SiOₓ/n-SiC/n-Si Resistive Nonvolatile Memory

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Abstract
We have proposed a pn-diode-structured p-CuOₓ/SiOₓ/n-SiC/n-Si resistive nonvolatile memory, which has an excellent rectifying I-V characteristic because of its pn-diode principle behavior. The forward bias current changes between high and low currents, which corresponds to that the memory state changes between a low-resistive on state and a high-resistive off state, respectively. The on and off states are experimentally suggested to be caused depending on nonexistence or existence of trapped electrons at the defect states of the thin SiOₓ layer. This memory also shows good endurance characteristics of more than 10⁵ rewriting cycles. The pn-diode rectifying characteristic is suitable for a cross-point configuration memory cell array which is an ultimately high-dense memory cell arrangement.

1. Introduction
A resistive random access memory (ReRAM) is a promising nonvolatile memory (NVM), because it has a two-terminal structure and can be more densely integrated than current three-terminal-structured memory devices.

To integrate two-terminal memory cells densely, a cross-point configuration memory cell array is promising, which is an ultimately high-dense memory cell arrangement. In this configuration, however, misreading occurs by the reverse current through unselected memory cells. It is then important to arrange memory cells with an excellent rectifying characteristic.

In this paper, we have first proposed a pn-diode-structured p-CuOₓ/SiOₓ/n-SiC/n-Si two-terminal resistive memory cell which has originally a rectifying principle behavior. The CuOₓ is generally known to be p-type semiconducting oxide [1]. In this paper, we report the electric characteristics and memory functions, and discuss the memory device physics.

2. Experimental
Fig. 1(a) shows the structure of our proposed memory device. The n-type 3C-SiC layer was formed with 80 nm thickness on a 4° off-axis Si(111) substrate by our magnetron sputter method [2]. After formation of a very thin SiOₓ layer by thermal oxidation of the SiC surface layer at 1073 K for 60 min, a Cu film with 50 nm thickness was formed by vapor deposition method. And then, the Cu film was thermally oxidized at 473 K for 60 min (called sample A). For comparison, we prepared a device without a SiOₓ layer, as shown in Fig. 1(b) (called sample B).

Fig. 1. Structures of (a) our proposed Metal/p-CuOₓ/SiOₓ/n-SiC/n-Si(111)/Metal (sample A) resistive nonvolatile memory (NVM) and (b) Metal/p-CuOₓ/3C-SiC/n-Si(111)/Metal (sample B), which was prepared for comparison to device (a).

Fig. 2. XPS spectra obtained from Cu film and oxidized Cu film, which is formed by thermal oxidation of Cu at 473 K for 60 min.

Fig. 3. Typical I-V curves obtained from samples A and B.
3. Results and Discussion

3-1. XPS Cu oxide analysis and Static I-V behavior

We show XPS spectra of a Cu film and the Cu oxide film, formed by thermal oxidation of Cu at 473 K for 60 min, in Fig. 2. Formation of CuO is dominant in the oxidized Cu film [3]. We have further confirmed experimentally that the oxidized Cu is a p-type semiconductor.

![Fig. 4. Typical C-V curve obtained from sample A.](image)

Typical I-V curves of samples A and B are shown in Fig. 3. Sample A has a large hysteresis in the forward bias. On the other hand, sample B has no hysteresis, which indicates that the SiO_x layer relates to generation of the memory function. By contacting p-CuO_x to n-SiC/n-Si, an excellent rectifying behavior was obtained, which results from the pn-diode principle characteristics. Thus, this pn diode is a promising structure for the cross-point cell array.

3-2. C-V characteristic and memory operation mechanism

Fig. 4 shows a typical C-V characteristic measured at 100 kHz. The hysteresis loop generated in the forward positive bias indicates that trap states are acceptor-like and negatively charged by electron trapping. These traps are probably caused in the SiO_x layer, because the hysteresis appears only after the SiO_x layer formation, as described in section 3-1. The band diagrams, shown in Fig. 5, illustrate the memory function mechanisms, assuming CuO_x is CuO. The memory state changes between a low-resistive (on) and a high-resistive (off) state, depending on nonexistence (Fig. 5(2)) or existence (Fig. 5(1)) of trapped electrons at the defect states of the thin SiO_x layer.

![Fig. 5. Suggested memory function mechanisms for sample A.](image)

3-3. Dynamic behavior and endurance characteristics

Fig. 6 shows dynamic responses to a series of ‘erase’, ‘read’, ‘write’, and ‘read’ pulse operations with a pulse width of 20 µs. Sample A responses in µs order to the input pulses, and also exhibits a good endurance characteristics with more than 10^5 rewriting switching cycles with an on/off current ratio of more than ~20, as shown in Fig. 7.

![Fig. 6. Pulse response characteristic obtained from sample A.](image)

4. Conclusions

We have first proposed a pn-diode-structured p-CuO_x/SiO_x/n-SiC/n-Si two-terminal resistive memory. The device exhibits an excellent rectifying characteristic due to its original diode principle behavior and the forward bias current can be controlled between high and low currents, which correspond to a low-resistive on state and a high-resistive off state. The on and off states are experimentally suggested to be caused by nonexistence and existence of trapped electrons at the SiO_x defect states, respectively. The device shows excellent memory endurance characteristics of over 10^5 rewriting switching cycles with an on/off current ratio of ≥ ~20. This pn-diode resistive memory is expected to be applied to ultimately high-density memory cell array with a cross-point memory cell configuration.

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References