A-1-3

Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp412-413

Interface Engineering in Homogeneous Barrier Modulation RRAM for 3D Vertical Memory Applications

Wei-Li Lai[1], Chun-Tse Chou[1], Chung-Wei Hsu[1], Jen-Chieh Liu[1], Boris Hudec[1], Chia-Hua Ho[2], Wen-Yueh Jang[2], Chen-Hsi Lin[2] and Tuo-Hung Hou[1]

[1]Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
[2]Winbond Electronics Corporation, Taichung, Taiwan
*Tel:+886-3-5712121#54219;E-mail:larrysmsn1226@hotmail.com

Abstract

Promising RRAM device based on homogeneous barrier modulation (HBM) is further improved by replacing Ti BE with TiN, which has better immunity against oxidation and is also VLSI-compatible. The influence of larger band offset at TiO_2/TiN interface was quantitatively investigated. Finally, the issue is compensated by inserting a V_o-rich TiO_x buffer layer so the device keeps comparable memory performance.

1. Introduction

Previously, a novel $Ta/TaO_x/TiO_2/Ti$ resistive-switching random access memory (RRAM) featuring homogeneous barrier modulation mechanism has been proposed for ultra-high density 3D vertical memory architecture [1-2]. However, stacked Ti bottom electrodes (BEs) are easily oxidized when depositing insulating oxide layers, and this would become a significant issue as the Ti thickness scales down (Fig.1). An alternative approach to avoid this concern while keeping good device performance is necessary. In this work, TiN is introduced to replace the original Ti BE since TiN is an inert metal with respect to Ti and it is also compatible with nowadays VLSI technology. Furthermore, to facilitate resistive switching, an oxygen vacancy (V_o)-rich TiO_x interfacial layer is needed between TiO_2 and TiN to reduce the interfacial Schottky barrier.

2. Experiment Procedures

A 5-nm V_o-rich TiO_x layer was deposited by reactive DC sputtering on the TiN BE, followed by 30-nm stoichiometric TiO_2. For comparison, control samples on the TiN and Ti BEs without the TiO_x interfacial layer were also fabricated. Then, a 10-nm TaO_x layer was deposited on TiO_2/TiO_x/TiN and also on the TiO_2/TiN and TiO_2/Ti control samples. Finally, 100-nm thick Ta top electrodes with a radius of 100 μm were deposited using a shadow mask.

3. Results and Discussion

Fig. 2 compares the DC *I-V* curves of the $Ta/TaO_x/TiO_2$/Ti and $Ta/TaO_x/TiO_2$/TiN samples. In contrast to the distinct memory window of the $Ta/TaO_x/TiO_2$/Ti RRAM, there is no observable resistance change under both positive and negative bias in the $Ta/TaO_x/TiO_2$/TiN control sample. To obtain more insight, the TiO_2/Ti (BE) interface of the $Ta/TaO_x/TiO_2$/Ti stack was investigated. An interfacial V_o-rich TiO_x layer was found between TiO_2 and Ti using TEM and XPS analyses (Fig. 3). The influence of the TiO_x layer on the Schottky barrier height was quantitatively investigated by adding an interfacial TiO_x layer between TiO_2/TiN and measuring Pt/TiO_2/TiN and $Pt/TiO_2/TiO_x$/TiN diodes at 25 to 100 ℃. The extracted Schottky barrier height at the TiO_2 /TiN interface is around 0.6 eV at zero bias (Fig.5). On the other hand, TiO_2/TiO_x/TiN interface shows a lowered barrier height of 0.21 eV, which is close to 0.2 eV of TiO_2/Ti [3]. This result infers that the TiO_x V_o-rich layer can effectively reduce the Schottky barrier height at the TiO_2/TiN interface.

The importance of reducing Schottky barrier height at the bottom interface is still under investigation. According to our previous study on the HBM RRAM, the high resistance state (HRS) and low resistance state (LRS) are attributed to the modulated Schottky barrier at the Ta/TaO_x interface because of the oxygen ion migration in TaO_x. Sufficient voltage drop on TaO_x is necessary to drive oxygen ions toward/against Ta top electrode and render resistive switching. However, the higher Schottky barrier at TiO_2/TiN interface could suppress the resistive switching since the band mismatch at the TiO_2/TiN interface is much higher than 0.2 eV of the TiO_2/Ti interface [3]. The more Ohmic-like TiO_2/Ti interface ensures that most of the SET voltage drops on TaO_x. By contrast, a significant portion of SET voltage drops at the Schottky TiO_2/TiN interface, as illustrated in the simplified equivalent circuits of Fig. 6.

Finally, the $Ta/TaO_x/TiO_2/TiO_x$/TiN RRAM was examined, showing desirable characteristics such as stable bipolar resistive-switching (BRS) with clear memory window (Figs. 7-9), stable self-rectifying ratio (I_{LRS}@-2V/I_{LRS}@2V) up to 4 orders of magnitude (Fig. 10), and multi-level operation (Fig. 11). However, the retention of this RRAM cell still needs to be improved (Fig.12).

4. Conclusions

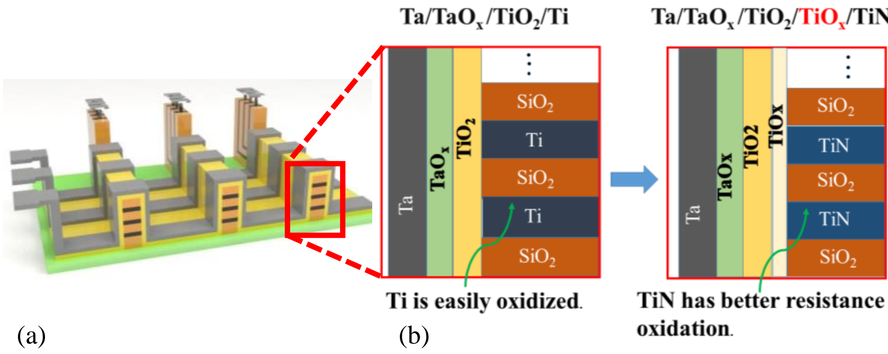
In summary, by adding a TiO_x V_o-rich inter-layer in $Ta/TaO_x/TiO_2/TiO_x$/TiN RRAM the Schottky barrier at TiO_2/TiN interface can be reduced and Ti bottom electrode can be replaced by VLSI-compatible, highly scalable TiN. Such a RRAM structure still possesses highly desired features including: (1) forming-free, (2) compliance-free, (3) stable BRS (4) multi-level operation (5) self-rectifying ratio up to 4 orders, all of which are essential for integration in future high-density crossbar and 3D vertical RRAM arrays.

Acknowledgement

B. Hudec acknowledges the financial support of International Visegrad Fund. T.-H. Hou acknowledges support in part by NCTU-UCB I-RiCE program, under grant MOST 103-2911-I-009-302.

References

[1] C.-W. Hsu et al., in *Nanotechnology*, 2014, pp. 25.16: 165202.
[2] C.-W. Hsu et al., i*n Symp. on VLSI Tech.*, 2013, pp. T166-T167.
[3] J.-J. Huang et al., in *Applied Physics Letters*, 2010, pp. 96.26: 262901.



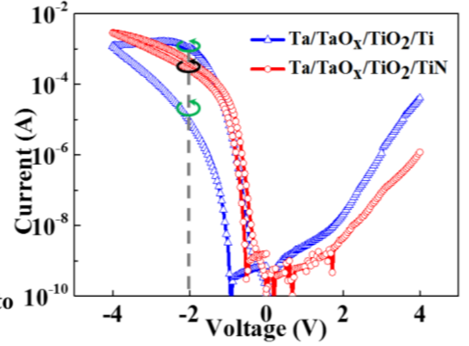


Fig.1. (a) Sketch of the $Ta/TaO_x/TiO_2/Ti$ 3D vertical RRAM array [2]. (b) 3D vertical RRAM cell structure zoom-up with both the $Ta/TaO_x/TiO_2/Ti$ and $Ta/TaO_x/TiO_2/TiO_x/TiN$ unit cells. The Ti BE is replaced with TiN in this work.

Fig.2. I-V curves of $Ta/TaO_x/TiO_2/TiN$, showing no resistive switching as compared with $Ta/TaO_x/TiO_2/Ti$.

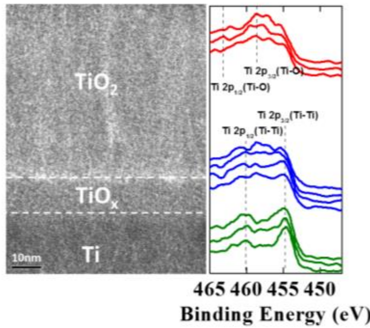


Fig.4. TEM cross-sectional image and corresponding XPS depth profiles of the TiO_2/Ti interface. A TiO_x interfacial layer exists between Ti and TiO_2.

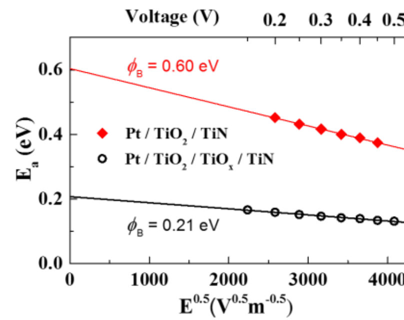


Fig.5. Extracted barrier heights between $TiO_2(/TiO_x)$ and TiN from temperature-dependent Schottky-emission fittings of the $Pt/TiO_2(/TiO_x)/TiN$ diodes.

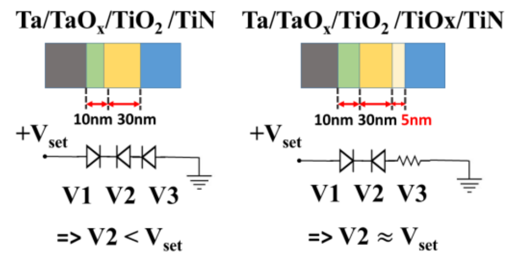


Fig.6. Equivalent circuit of $Ta/TaO_x/TiO_2/TiN$ and $Ta/TaO_x/TiO_2/TiO_x/TiN$ at V_{SET}. Resistive switching works if the voltage drop of V2 is high enough.

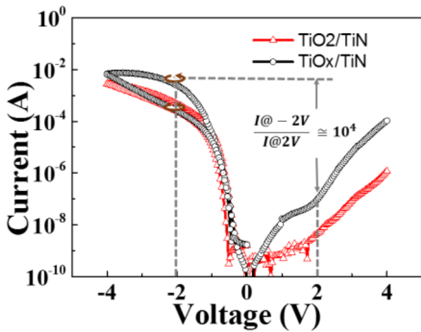


Fig.7. BRS and self-rectification of the $Ta/TaO_x/TiO_2/TiO_x/TiN$ RRAM stack.

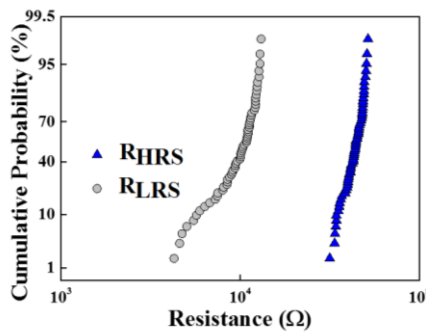


Fig.8. Resistance cumulative probability plot in HRS&LRS of the $Ta/TaO_x/TiO_2/TiO_x/TiN$ stack.

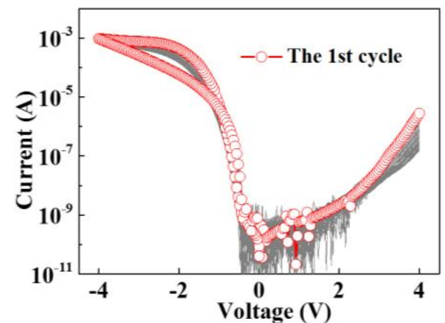


Fig.9. $Ta/TaO_x/TiO_2/TiO_x/TiN$ stack showing stable BRS for more than 100 DC switching cycles.

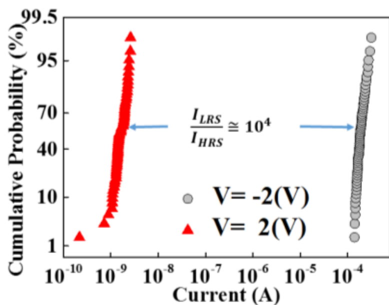


Fig.10. Cumulative probability plot of LRS current at +2 and -2 V in the $Ta/TaO_x/TiO_2/TiO_x/TiN$ stack, showing a stable self-rectification ratio of 10^4.

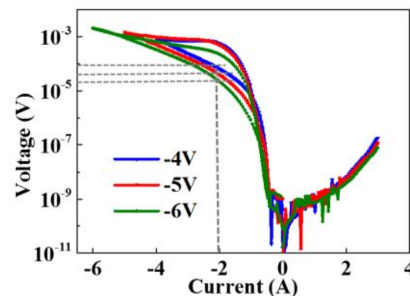


Fig.11 MLC operation by using various V_{RESET} at -4, -5, and -6 V in the $Ta/TaO_x/TiO_2/TiO_x/TiN$ stack.

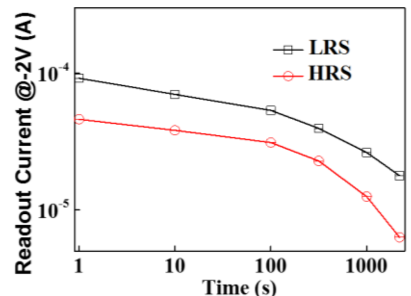


Fig.12. LRS and HRS retention of the $Ta/TaO_x/TiO_2/TiO_x/TiN$ stack at room temperature.