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Electro-thermal driven nano-scale IMT characteristics of $SmNiO_3$ for selector application of cross-point memory array

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1. Introduction

To implement cross-point memory array, we need to develop non-linear selector devices which can solve the sneak path current problem [1]. Many devices with insulator to metal transition (IMT) are proposed (shown in Fig. 1) as a good selector device. But some of them are suffering from low transition temperature or high processing temperature which are not useful for memory application [3]. Recently, $SmNiO_3$, which exhibits high transition temperature (~130^{o}C) was investigated as an alternative IMT materials [4]. The main challenge to stabilize $SmNiO_3$ (SNO) is the stabilization of Ni^{3+} ion in the NiO_6 octahedra which needs enough oxygen. To stabilize Ni^{3+} ion in SNO, high pressure oxygen annealing at high temperature is required, which is not practical for high density memory application [4].
In this paper, we propose an alternative and practical technique to stabilize Ni^{3+} ion by applying negative electric bias which can increase oxygen concentration in the bottom electrode regions of $SmNiO_x$ film in Pt /$SmNiO_x$/ Pt structures. The 1S1R characteristics are also analyzed with Ta_2O_5 based ReRAM.

2. Experimental:

Pt /$SmNiO_x$/Pt device was fabricated by using 250 nm via-hole structure. Fig. 2 shows the BEOL compatible febrication process flow with the schametic device stack. 12 nm $SmNiO_x$ is deposited by using RF magnetron sputtering at ~300^{o}C with ~3% oxygen of (Ar+O_2) mixture following top Pt sputtering.

3. Result & Discussion

The current voltage characteristics of Pt/$SmNiO_x$/Pt device is shown in Fig. 3. The negative bias forming turns the device from insulating to metallic state. The XPS analysis confirms the presence of different valence states of Sm and Ni (855.6 eV for Ni^{3+} & ~854.4 eV for Ni^{2+}) (Fig. 4). These different valence states of Sm and Ni indicate that, several sub-oxides may present like Sm_2O_3, SmO, NiO along with SNO in the as deposited oxide film [5]. The probable mechanism for insulator to metal transition of Pt/$SmNiO_x$/Pt device is shown in the Schematic Fig. 5. By increasing the negative voltage, during forming, the oxygen ion migration from top to bottom electrode region can be increased (Fig. 5 (a)). Due to this reason, the region near the top and bottom electrode interface will be enriched by oxygen-vacancy and oxygen-ion respectively. These oxygen-vacancy rich region will form conducting filament. Furthermore, due to the electric field and the conducting filament, the temperature of a narrow region near bottom electrode will be increased because of joule heating effect [6]. These excess oxygen ions at high temperature stabilize Ni^{3+} ions and form stable SNO phase which generates localized IMT characteristics for the subsequent voltage pulse (Fig. 5(b)). Also, Fig 6 shows that, by increasing the measurement temperature, the oxygen ion migration can be accelerated which reduces required electric field and hence forming voltage (V_f) and V_{th} are decreased [7]. Further, the effect of different top electrodes are also investigated (shown in Fig. 7). The reactive top electrode W decreases O_2 ion from the oxide film and causes lack of O_2 to stabilize SNO during forming. This device shows nonlinear or memory characteristics. As TiN less reactive than W and more reactive than Pt it shows IMT by high power supply while Pt shows low power IMT. Fig. 8,9,10 show Uniform current distribution, good AC pulse endurance (>10^5 cycles @ 1 μs pulse width) in linear and log scale respectively which proves the excellent performance of the device. Again, at 85^{o}C, the device showed stable characteristics without any degradation for more than 10^4 s (shown in Fig. 11).
The 1S1R characteristics prove the feasibility of the device in the application (Fig. 12, 13); it decreases the leakage current at the ½ V_{read} and can be used successfully in memory-array. Fig 14 and 15 show the very controlled distribution of On-Off resistance and the current respectively at both V_{read} and ½ V_{read}.

4. Summary:

By introducing simple negative bias forming, the stabilization of localized $SmNiO_3$ is achieved due to the oxygen ion accumulation in the bottom electrode region. The electric power produces sufficient temperature to change the state from insulator to metal for the subsequent pulses after forming. This simple technique might be useful for $SmNiO_3$ as an IMT select device. Good uniformity in current distribution, thermal stability and switching endurance (> 10^5) also showed the feasibility of the device for selection application. Excellent 1S1R characteristics supports the device to use as a very good selector.

Acknowledgements:

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References: [1] M. Aono et al., Nat. Mater. **6**, (2007)833. **[2]** K szotet al., Nanotech. 22, (2011) 254001. **[3]** H. Hwang et al., IEEE Electron Device Lett. **33**, (2012)718. **[4]** S. Ramanathan et al., J. Mater. Chem. C.**1**, (2013)2445. **[5]** S. Ramanathan et al., J. Appl. Phys. **109**, (2011)124110. **[6]** B. I. Ryu et al., Appl. Phys. Lett. **88**, (2006)202102 **[7]** C.-Y. Lu et al., VLSI Symp. Tech. Dig., (2013) 100.

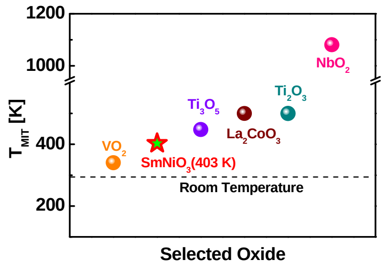

Fig.1 Different IMT devices with the transition temperatures. [2]

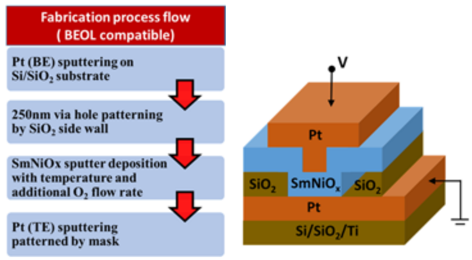

Fig.2 Device fabrication process flow and the schematic device structure.

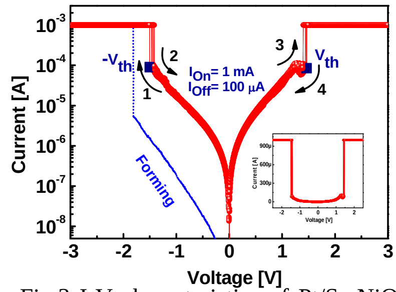

Fig.3 I-V characteristics of Pt/SmNiOx/Pt device. Inset shows the linear curve

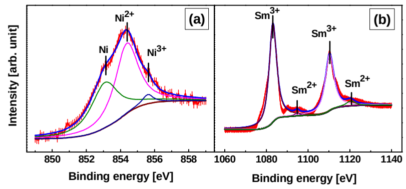

Fig.4 The XPS depth profiling spectra and deconvolution results of (a) Ni 2p and (b) Sm 3d core level in the bulk region after sputter etching.

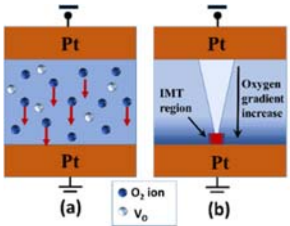

Fig.5 Schematic illustration of the proposed mechanism.(a) during –ve voltage forming O_2 ion migration from top to bottom and (b) localized IMT region formed at V_{th}.

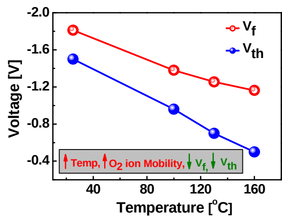

Fig.6 Temperature effect on the forming voltage and threshold voltage. Both are decreased with increasing measuring temperature.

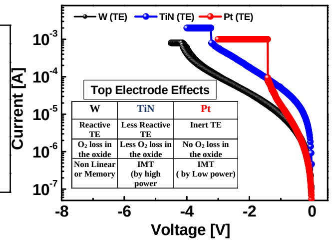

Fig.7 Different top electrode shows different characteristics which is also partially supports the proposed mechanism.

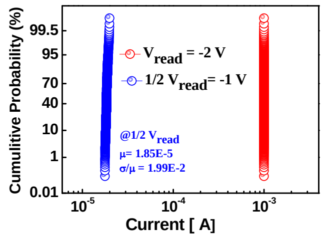

Fig.8 Uniform current distribution at read and ½ read voltage.

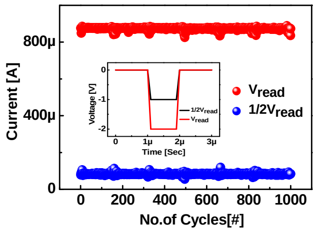

Fig.9 AC pulse endurance for first 10^3 cycles shows very uniform characteristics.

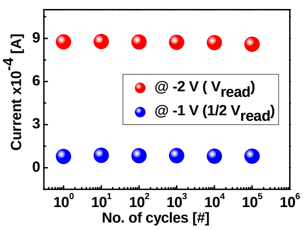

Fig.10 AC pulse endurance upto 10^5 cycles in log scale.

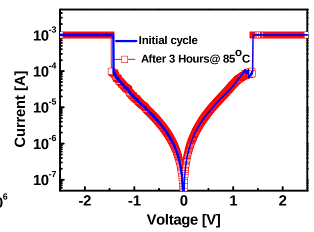

Fig.11 Thermal stability at 85 °C for more for more than 10^4 s without any degradation.

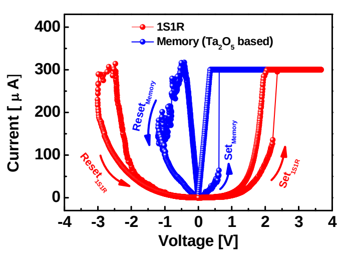

Fig.12 I-V characteristics of 1R and 1S1R devices. 1S1R significantly reduces the leakage current at lower voltage of 1R device.

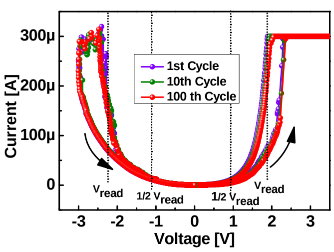

Fig.13 Multiple cycles of 1S1R device with read and ½ read voltage scheme.

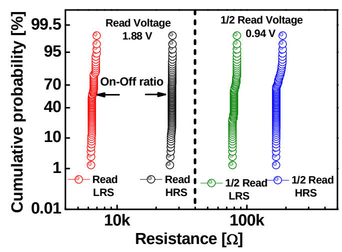

Fig.14 Uniform resistance distribution for read and ½ read voltage of the 1S1R device.

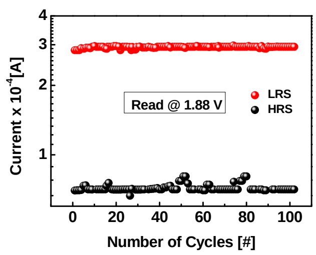

Fig.15 Current distribution of LRS and HRS at read voltage of 1S1R device.