Self-Rectifying Ta/TaO$_x$/TiO$_2$/Ti Cell for High-Density Flexible RRAM

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Abstract

A self-rectifying flexible RRAM has been successfully fabricated at low temperature on a plastic substrate using a fabrication-friendly Ta/TaO$_x$/TiO$_2$/Ti structure. In addition to the excellent flexible characteristics, the maximum array size is estimated exceeding 10 Mb by using an all-line pull-up read scheme.

1. Introduction

Flexible electronics is now under active development because of its low cost, flexibility, and light weight [1]. Among several emerging non-volatile memories, crossbar RRAM seems an ideal candidate to be integrated in flexible electronics because of its low process temperature and simple structure. However, crossbar RRAM suffers from severe read errors in large arrays because of the sneak current flowing through the unselected bits. A nonlinear device can be integrated with a linear RRAM in a metal-insulator-metal-insulator-metal (MIMIM) structure to suppress sneak current, such as one selector-one resistor (1S1R) [2] and one diode-one resistor (1D1R) (Fig. 1). However, adding additional nonlinear devices inevitably complicates the fabrication. This is particularly critical for flexible electronics because its fabrication technique is less matured. To simplify the fabrication of the flexible RRAM, a Ta/TaO$_x$/TiO$_2$/Ti self-rectifying RRAM that achieves both stable resistive switch (RS) and nonlinearity current-voltage characteristics [3] simultaneously was fabricated at low temperature on a flexible polyimide (PI) in this study. At least one photolithography and one metal patterning steps are saved in this MIIM cell as compared with the previous MIMIM cells (Fig. 1). This self-rectifying RRAM cell shows promising flexible characteristics and great potential of realizing a large array size exceeding 10 Mb using an all-line pull-up (All-LPU) read scheme.

2. Experimental Procedures

A SiO$_2$ layer of 50 nm was deposited by chemical vapor deposition (CVD) on a flexible polyimide (PI) as an adhesion layer. A bilayer Ti/Ni bottom electrode (Ti on the top) was deposited on SiO$_2$ by DC sputtering. As for the self-rectifying RRAM element, 20-nm TaO$_x$ and 60-nm TiO$_2$ were deposited on the bottom electrode by reactive magnetron DC sputtering. Finally, the Ta top electrodes were defined by a shadow mask. All deposition processes were finished at room temperature. The robustness of the self-rectifying flexible devices under mechanical bending strain are clearly shown in Fig. 2.

3. Results and Discussion

Fig. 3 illustrates the electrical characteristics of the self-rectifying RRAM at the flat state. SET and RESET occur at positive and negative polarities, respectively, with a maximum operating current below 1 µA. When applying a positive voltage sweep, the current is suppressed below 1 nA from 0 to +3 V. When applying a negative voltage sweep, the resistance ratio of the high resistance state (HRS) and low resistance state (LRS) about 10 can be clearly distinguished at a read voltage of -2 V. In addition, the self-rectification ratio of LRS at ±2 V is more than 100. Although both the HRS and LRS currents reduce at the bending state with a bending radius of 30 mm, the HRS and LRS resistance ratio still maintains around 10, as shown in Fig. 4. By contrast, the self-rectification ratio of LRS at ± 2 V degrades to 10 under bending, as shown in Fig. 5, because the currents at +2 V and -2 V are increased and decreased, respectively. Under different bending radii, the resistance ratios remain stable, as illustrated in Fig. 6. Fig. 7 demonstrates the data retention time exceeds 10^4 s either at the flat or bending state. Furthermore, a mechanical bending vehicle shown in Fig. 8 was used to test the device robustness under repeated bending cycles. Fig. 9 shows that both the HRS and LRS are stable after 10^3 bending cycles.

Fig. 10 shows a typical linear Ta/TaO$_x$/Pt RRAM for comparison. To analyze the maximum array size in a *NxN* crossbar array, the All-LPU scheme was utilized because it minimizes the sneak current in large crossbar arrays [4]. As shown in Fig. 11, unselected bit and word lines are all pulled up, and the sneak current path is indicated by the blue arrows. For the worst-case read scenario, both selected cell (R_{sel}) and region 1 are at HRS or at LRS in the same time [4]. The read margins may be calculated by *SPICE* numerical simulation. The results of the proposed self-rectifying RRAM and the typical linear RRAM shown in Fig. 10 are compared in Fig. 12. The self-rectifying RRAM performed much better than the linear RRAM, and the estimated array size is more than 10 Mb at a 10% read margin.

4. Conclusion

The Ta/TaO$_x$/TiO$_2$/Ti self-rectifying RRAM was successfully fabricated on a PI substrate at room temperature. Although its self-rectification ratio degrades slightly, the resistance ratio remains stable while bending. Combining the All-LPU read scheme, the proposed self-rectifying RRAM allows a projected maximum array size exceeding 10 Mb without read error.

References

[1] T. Jackson et al., in IEDM Tech. Dig., 2005, pp. 438–441.

[2] J. J. Huang et al., in IEDM Tech. Dig., 2011, pp. 733-736.

[3] C. W Hsu et al., in VLSI Technology, 2013, pp. T166-T167.

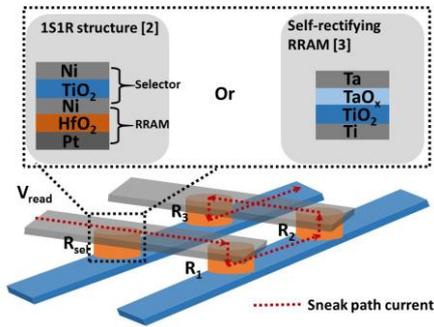[4] C. L. Lo et al., in 2013, in VLSI-TSA, 2013, pp. 40-41.

Fig. 1 Either 1D1R and 1S1R cells in a MIMIM structure or a self-rectifying RRAM in a MIIM structure can be used to solve the sneak current issue in the crossbar array.
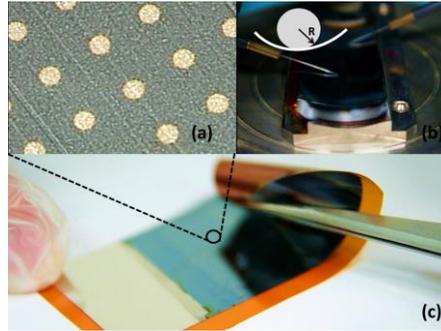

Fig. 2 (a) Optical microscope image of the fabricated RRAM devices. (b) Electrical measurement of the RRAM device under a mechanical bending strain with a 30-mm bending radius. (c) Image of the flexible RRAM.
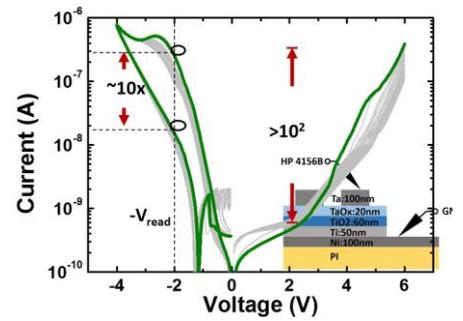

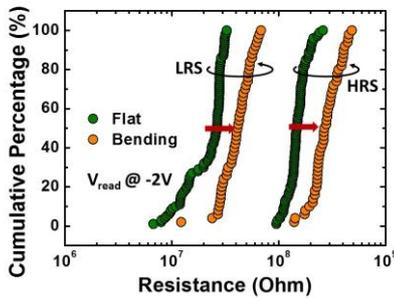**Fig. 3** Current-voltage characteristics of the self-rectifying RRAM at the flat state.

Fig. 4 Cumulative percentage of resistance states (HRS & LRS @ -2 V) of the self-rectifying RRAM at both the flat and bending states.
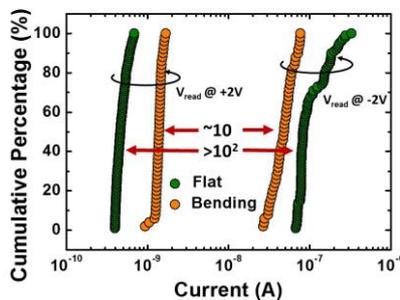
Fig. 5 Cumulate percentage of LRS current levels of the self-rectifying RRAM at read voltages of ±2 V at both the flat and bending states.
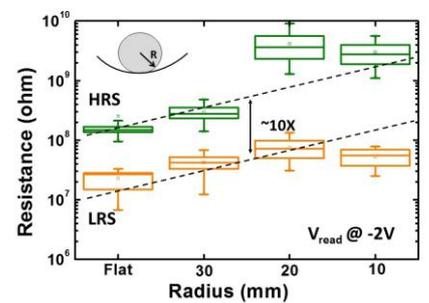

Fig. 6 Resistance distribution at a read voltage of -2 V at the bending states with different bending radius.
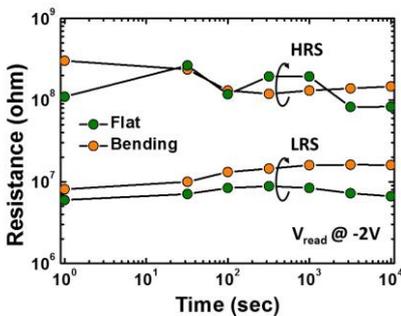

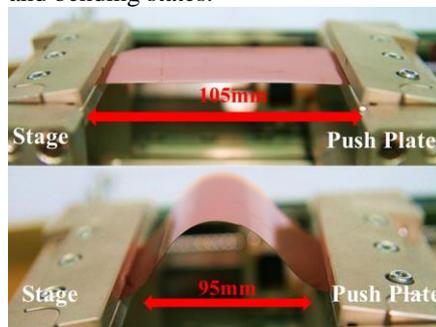**Fig. 7** Excellent retention time of HRS and LRS at both the flat and bending states.

Fig. 8 Mechanical bending vehicle used to test the device robustness under repeated bending cycles.
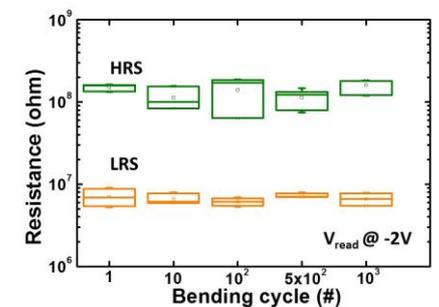

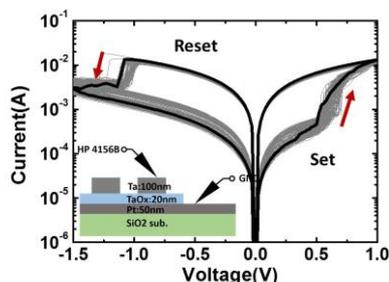**Fig. 9** HRS and LRS exhibit excellent robustness after 10^3 repeated bending cycles.

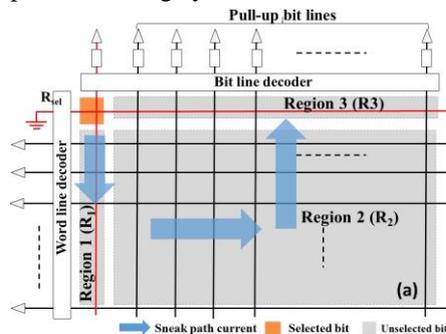**Fig. 10** *I-V* characteristics of a linear Ta/TaO$_x$/Pt RRAM.

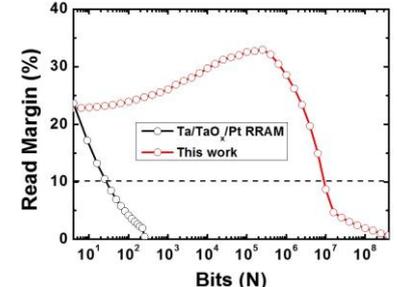**Fig. 11** All-LPU read scheme for a $N \times N$ crossbar array.

Fig. 12 Read margin calculated by SPICE numerical simulation for the linear and self-rectifying RRAM.