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Modeling of Read Disturbance Mechanism due to Carrier Trapping in Sub-20nm NAND Flash Memory

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Abstract

We observed an increase of V_{th} (charge gain) by read disturbance mechanism at PV1 and ERS states in retention characteristics of sub-20nm NAND Flash main-chip. As a result, we quantitatively modeled read disturbance mechanism by the amount of final ΔV_{th} and deterioration coefficient α which is related to the number of read operation times. It was also observed that those parameters increase with increasing cycling times and have larger value at ERS state than that at PV1 state.

1. Introduction

As NAND Flash memory has been scaled down for high density, reliability issues have become critical problems [1]-[2]. For detailed analysis of main reason affecting retention issues, we proposed the method to separate dominant failure mechanisms related to traps (the detrapping mechanism [3], the trap-assisted tunneling mechanism (TAT) [4] and interface trap recovery mechanism (Nit recovery)) [5].

In this paper, we analyzed the behavior of threshold voltage variation (ΔV_{th} = $V_{th,initial}$ - $V_{th,after\ bake}$) and deterioration coefficient α of read disturbance mechanism observed at PV1 and ERS in sub-20nm NAND Flash memory. Read disturbance increases the number of bits moved to higher states (PV2 and PV1) whenever read operation is performed. To predict accurate life time at PV1 and ERS states in NAND Flash memories, this characteristic should be analyzed carefully.

2. Results and discussions

Figure 1(a) shows the schematic of NAND Flash memory array during read operation. Read disturbance occurs at the cells where V_{pass} is applied. Figure 1(b) shows the trapping process of the electrons contributing to read disturbance. Although the V_{pass} is not large enough to generate tunneling, some electrons are injected to the trap-sites near the Si-SiO2 interface and increase V_{th}. Since this process occurs only during read operation, the charge gain behavior due to read disturbance only depends on read operation times and the amount of empty trap sites. As shown in Fig. 1(c), since V_{th} at PV1 and ERS states is smaller than that at other states, small pass bias can induce large electric field across tunneling oxide layer ((Vpass - Vth)/Tox) enough to cause the electrons to be tunneled to the border trap-sites in the oxide layer [6]. In this paper, the charge behaviors are extracted by observing the data point where the probability level is 1% in the distribution of V_{th} as shown in Fig. 1(c).

Based on the proposed model [7]-[9], read disturbance is added as the new mechanism as shown in (1).

$$\Delta V_{th\_TOTAL} = \Delta V_{th\_Det}\cdot\left[1-\exp\left(-\left(\frac{t_R}{\tau_{Det}}\right)^{\beta_{Det}}\right)\right]+\Delta V_{th\_N_{it}}\cdot\left[1-\exp\left(-\left(\frac{t_R}{\tau_{N_{it}}}\right)^{\beta_{Nit}}\right)\right]$$
$$+\Delta V_{th\_TAT}\cdot\left[1-\exp\left(-\left(\frac{t_R}{\tau_{TAT}}\right)^{\beta_{TAT}}\right)\right]+\Delta V_{th\_READ}\cdot\left[1-\exp\left(-(\alpha\cdot n)^{\beta_{READ}}\right)\right] \quad (1)$$

$\Delta V_{th(mechanism)}$ and τ are the amount of charge (loss or gain) and time constant of each mechanism, respectively. β is the parameter determining the increasing shape of charge loss (gain) model (1) [9]. Unlike other mechanisms, read disturbance is modeled as the function of n, the cumulative number of read operation. α is deterioration coefficient and characterizes the increasing rate of read disturbance. All parameters are extracted by fitting measurement data with model iteratively [7]-[9].

The inset of Fig. 2(a) shows the cumulative number of read operation according to baking time at two temperature range used in our measurement. From this figure, the read disturbance mechanism quantitatively modeled as a function of cumulative number of read operation can be expressed in bake time domain as shown in Fig. 3. Figure 2(a) shows the simulated charge gain behavior due to read disturbance extracted from 5K cycled PV1 state at 40°C. At the first read operation, since there are many empty trap-sites in tunneling oxide layer, the amount of charge gain is the largest. As read times increases, the incremental amount of charge gain decreases gradually and becomes saturated due to the limited number of trap-sites. Figure 2(c) shows the energy band diagram during the bake time. At PV3 and PV2 states, since the electric field at tunneling oxide layer is applied toward the substrate, electrons trapped at border trap-sites can be tunneled out directly to the substrate after read operation is over. However, since the distance between the floating gate and the border trap-sites is too large for electrons to be tunneled directly and the energy level of trap sites is too deep to be thermally excited at PV1 and ERS states, trapped electrons are rarely tunneled out to the floating gate during the bake time.

Figure 3 shows the charge behavior (loss or gain) at PV1 and ERS states in 5K cycled NAND Flash main-chip according to the bake time. It is observed that N_{it} recovery and detrapping mechanisms are served as the charge loss while read disturbance and TAT mechanisms contribute to the charge gain [9]. Since the charge gain due to read disturbance occurs only during read operation, the charge loss and gain behavior can occur alternately between measured data. Since various failure mechanisms have different temperature dependency, total charge behavior is different according to baking temperature.

Figure 4(a) shows the amount of final ΔV_{th} in read disturbance mechanism at PV1 and ERS states according to the number of

cycling operation. Since the number of empty border trap-sites in tunneling oxide layer increases as cycling times increases, the amount of charge gain also increases at both states. At ERS state, the charge gain is larger than that at PV1 state because lower V_{th} causes a stronger electric field across tunneling oxide layer. Figure 4(b) shows the deterioration coefficient α at PV1 and ERS states according to the number of cycling operation. As cycling times increases, since newly generated trap-sites lower the electric energy barrier for the electrons to be injected to trap-sites easily, the deterioration coefficient α increases.

Figure 5(a) and (b) are the charge loss and gain behavior simulated by (1) up to 10 years at PV1 and ERS states. With the read operation in this measurement, the unwanted charge gain component by disturbance is added to the intrinsic charge behavior and it prevents the performance of NAND Flash main-chip from being evaluated accurately at PV1 and ERS states. Therefore, to estimate accurate life-time of NAND Flash main-chip in itself, the component by read disturbance at PV1 and ERS states should be carefully removed.

3. Conclusions

We extracted the final ΔV_{th} and deterioration coefficient α of read disturbance mechanism at PV1 and ERS states in NAND Flash main-chip. Read disturbance deteriorates the retention characteristics by increasing the V_{th} whenever read operation is performed. For accurate life-time prediction of NAND Flash main-chip in itself, the component by read disturbance mechanism should be removed

Acknowledgements

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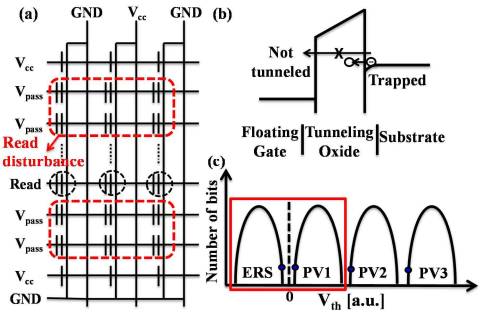

Fig. 1. (a) The schematic of NAND Flash memory array during read operation. (b) is the concept of electron trapping process to border trap-site contributing to read disturbance mechanism. (c) is the distribution of V_{th} at each state.

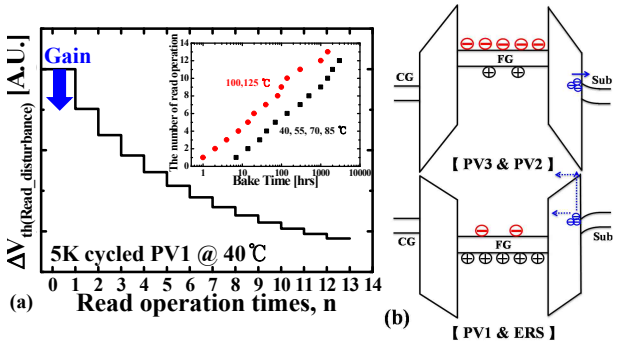

Fig. 2. (a) The charge gain behavior simulated by read disturbance model in 5K cycled PV1 state at 40°C in read operation times domain. The inset shows the cumulative number of read operation according to baking time at two temperature regime. (b) shows the energy band diagram during the bake operation at each state.

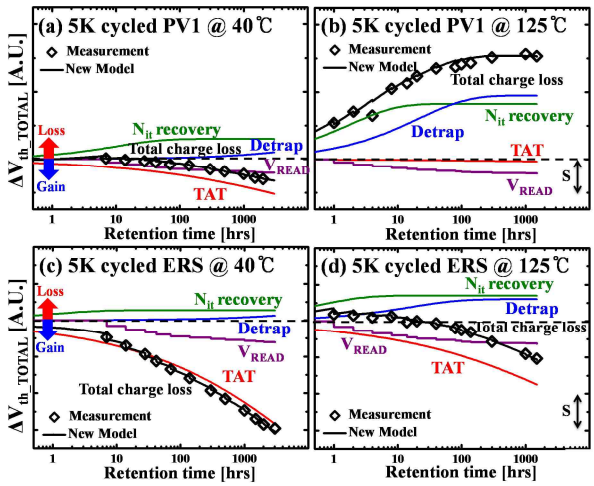

Fig. 3. The charge (loss or gain) behavior at PV1 and ERS states in 5K cycled NAND Flash main-chip. S is the same scale unit of ΔV_{th} to compare the charge loss/gain in the PV1 and ERS states. Open symbols are measured data and solid lines are simulated by (1).

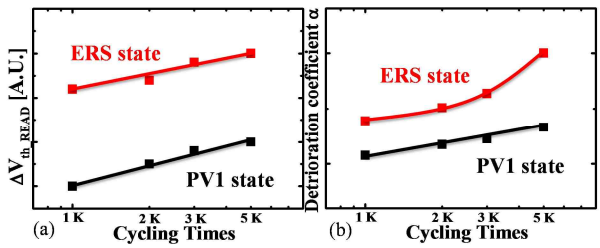

Fig. 4. (a) The amount of final ΔV_{th} and (b) deterioration coefficient α in read disturbance increase with increasing cycling times.

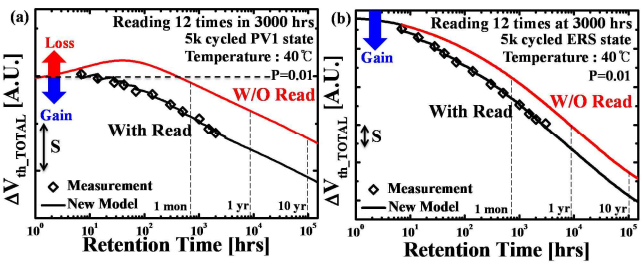

Fig. 5. The charge (loss or gain) behavior simulated by $\Delta V_{th(Total)}$ in (1) at 40℃ up to 10 years in (a) PV1 and (b) ERS states.