

DRAM with Storage Capacitance of 3.9 fF using CAAC-OS Transistor with L of 60 nm and having More Than 1-h Retention Characteristics

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Abstract

The dynamic oxide semiconductor random access memory (DOSRAM) array that achieves reduction in storage capacitance and power consumption has been fabricated using a c-axis aligned crystalline oxide semiconductor (CAAC-OS, a crystalline oxide semiconductor) transistor with $L = 60$ nm having extremely low off-state current. We confirmed that this array composed of cells each including a CAAC-OS transistor with $W/L = 40$ nm/60 nm using InGaZnO and a 3.9-fF storage capacitor operates with a write time of 5 ns and a read time of 5 ns. This means that DOSRAM makes ensuring sufficient storage capacitance easier while maintaining the operation speed comparable to that of dynamic random access memory (DRAM). Furthermore, we found that the retention time of this array is more than 1 h, which is extremely longer than that of DRAM. Thus, DOSRAM is a promising replacement for DRAM.

1. Introduction

Dynamic random-access memory (DRAM), which is widely used in information equipment, should have high memory capacity and low power consumption. A problem in scaling DRAM to increase memory capacity is to ensure sufficient storage capacitance (C_s). A stack-type cell, conventionally employed in DRAM, has a storage capacitance of approximately 20 fF [1]; however, the formation of the cell becomes difficult with miniaturization because the aspect ratio is increased. Furthermore, DRAM, which is volatile memory, has to refresh data to hold data at intervals of 64 ms even in standby mode [1]. This refresh operation makes the reduction of power consumption difficult.

We believe that dynamic oxide semiconductor random access memory (DOSRAM) [2] can achieve two objectives: reduction in C_s and reduction in power consumption. In this paper, we demonstrate that these objectives can be achieved using a DOSRAM array that includes a c-axis aligned crystalline oxide semiconductor (CAAC-OS, a crystalline oxide semiconductor) transistor with $L = 60$ nm constructed using InGaZnO.

2. DOSRAM Cell

Like DRAM, the DOSRAM cell has a 1T1C cell structure (Fig. 1) and is expected to be fabricated to have a memory area of $6 F^2$. The DOSRAM can hold data for

longer than 10 days because of the extremely low off-state current of the CAAC-OS transistor [3,4]. Fig. 2 shows the I_d - V_g characteristics of the CAAC-OS transistor with $W/L = 40$ nm/60 nm. According to the graph, the off-state current is less than the measurement limit. Thus, it is expected that DOSRAM using such a miniaturized CAAC-OS transistor can be fabricated.

3. Strategy

We developed the following strategies to obtain the DOSRAM that can achieve C_s reduction and reduction in power consumption in refresh operations.

C_s Reduction

To reduce C_s in DOSRAM, the following two requirements should be satisfied.

First, data loss because of current leakage should be prevented. Because the CAAC-OS transistor with $L = 60$ nm has extremely low off-state current, it is expected that it has a sufficiently longer retention time than DRAM even when C_s is reduced.

Second, sufficient signal voltage (V_{sig}) during data reading should be ensured. To reduce C_s while ensuring necessary V_{sig} , bit line (BL) capacitance is reduced. As illustrated in Figs. 3(a) and 3(b), decreasing the number of memory cells per BL (N_{mc}/BL) in a DRAM array using silicon and shortening BL while maintaining memory capacity increase the area of a chip. In contrast, DOSRAM can be stacked over a sense amplifier formed using silicon as illustrated in Fig. 3(c). Such a structure enables N_{mc}/BL and C_s to be reduced without increasing the chip area.

Reduction in Power consumption in Refresh Operation

The long retention time of DOSRAM can decrease the refresh rate; thus, power consumption in refresh operations can be reduced.

4. Fabrication of Test Circuit

Fig. 4 shows a block diagram of test circuit. All the transistors in the circuit are CAAC-OS transistors constructed using InGaZnO. Each memory cell is composed of a CAAC-OS transistor with $W/L = 40$ nm/60 nm and a 3.9-fF storage capacitor. The value 3.9 fF is approximately one-fifth the C_s of DRAM. The memory array is an open BL type array with $N_{mc}/BL = 8$.

5. Results and Discussion

Figs. 5(a) and 5(b) show the operation waveforms of the fabricated test circuit. V_{sig} in the test circuit is obtained from ΔV in Fig. 5(b) and source follower

characteristics.

Next, the operation speed of the array was measured (Fig. 6). When both the write time and read time are longer than or equal to 10 ns, the value of V_{sig} increases no further and is greater than 200 mV. When both the write time and read time are 5 ns, the range of V_{sig} is narrow; nevertheless $V_{sig} \geq 100$ mV is satisfied.

Fig. 7 shows the retention characteristics of the test circuit. There is almost no change in the value of V_{sig} even after 1 h, owing to the extremely low off-state current of the CAAC-OS transistor. Assume that the refresh cycle of DOSRAM is 1 h, this is 56250 times the refresh cycle of DRAM (64 ms). This implies that power consumption in a DOSRAM refresh operation can be reduced to 1/56250 of that in DRAM.

6. Conclusions

We confirmed that a DOSRAM array with $N_{mc}/BL = 8$ and $C_s = 3.9$ fF using a CAAC-OS (a crystalline oxide semiconductor) transistor with $L = 60$ nm can operate with a write time of 5 ns and a read time of 5 ns and can hold data for more than 1 h. The C_s 3.9 fF is approximately one-fifth that of DRAM and thus can make the fabrication of a storage capacitor easier. Moreover, it has been found that a retention time of more than 1 h allows power consumption in refresh operations to be reduced to less than 1/56250 of that of DRAM.

The above features indicate that DOSRAM is a promising replacement for DRAM.

References

- [1] <http://www.itrs.net/reports.html> - 2013 Edition.
- [2] T. Atsumi *et al.*, *Int. Memory Workshop* (2012) pp. 99-102.
- [3] S. Yamazaki *et al.*, *Proc. SID'12 Dig.*, (2012) pp. 183-186.
- [4] K. Kato *et al.*, *Jpn. J. Appl. Phys.*, **51** (2012) 021201.

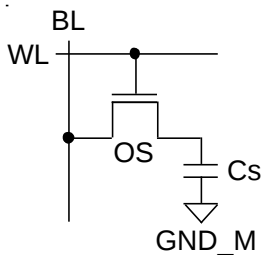


Fig. 1 DOSRAM cell structure

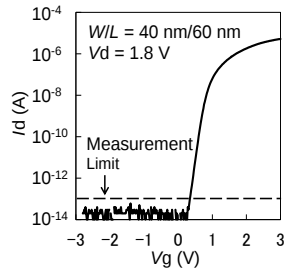


Fig. 2 I_d - V_g characteristics of CAAC-OS transistor

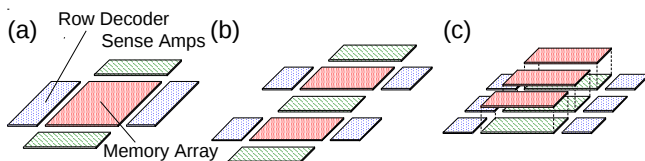


Fig. 3 Conceptual diagram of memory cell array

- (a) DRAM array (b) Separated DRAM arrays
(c) DOSRAM arrays arranged over sense amplifiers

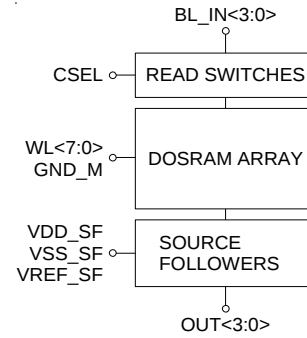


Fig. 4 Block diagram of test circuit

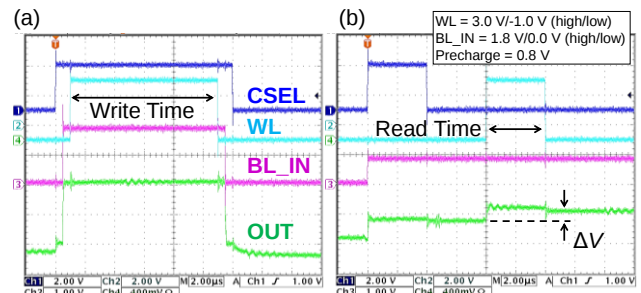


Fig. 5 Operation waveform chart of test circuit

- (a) Data "1" writing operation (b) Data "1" reading operation

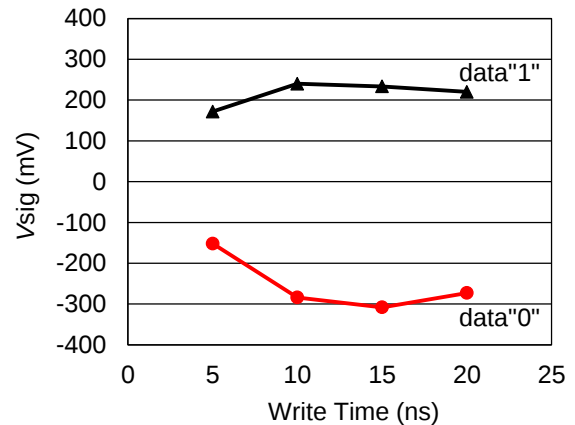


Fig. 6 Measurement results of operation speed (Read time = Write time)

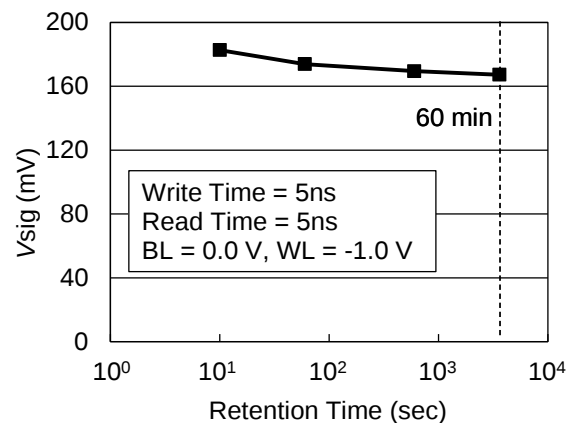


Fig. 7 Data "1" retention characteristics