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A 4F^2-cross-point Phase Change Memory Using Nano-crystalline Doped GeSbTe Material

Takahiro Morikawa, Kenichi Akita, Masaharu Kinoshita, Mitsuharu Tai, Takasumi Ohyanagi and Norikatsu Takaura

Low-power Electronics Association & Project,
West 7, 16-1 Onogawa, Tsukuba, Ibaraki 305-8569, Japan
Phone: +81-29-879-8262 E-mail: morikawa@leap.or.jp

Abstract

This paper reports on the fabrication and test results of 4F^2-cross-point phase change memory. The characteristics of a unipolar poly-Si diode with high drivability and low-power doped GeSbTe are presented. We also show selective reset/set in the array structure.

1. Introduction

To satisfy ever increasing demands for low-cost and high-speed storage, a variety of memory devices have been extensively investigated. Cross-point phase change memory (PCM) driven by a poly-Si diode is one of the most attractive technologies due to the simple fabrication process and small cell size [1, 2]. Issues of cross-point PCM are illustrated in Fig. 1. We previously reported a new phase change material with low thermal conductivity, nano-crystalline doped GST (nano-GST), which enables low-power programming and suppression of thermal disturbance [3]. In this paper, we report on the fabrication of cross-point test devices on a 300-mm wafer using the low-power material driven by the poly-Si diode [4]. The performances of the diode with high drivability and low-power programming and selective reset/set programming were demonstrated.

2. Device structure

The cross-point array structure shown in Fig. 2 was fabricated on a 300-mm Si wafer. To deposit the doped nano-GST material, co-sputtering of GST and a dielectric was utilized. Figure 3 shows the schematic view of test structure and the measurement setup. Four selectable cells are located in the center of the array, and the metal lines around them, which act as dummy lines, are connected with one another. The metal lines are selected by R/F matrix switches. In the DC measurements, SMUs measured the voltage and current of the selected bit line (BL) and word line (WL) with unselected BLs and WLs floating. In the pulse measurements, pulse generator (PG) 1 and 2 applied the voltage of a selected BL and unselected WLs, respectively. The pulse current was measured at the voltage of 50-Ohm termination in the oscilloscope.

3. Device test results

First, the performance of a diode is shown. Figure 4 shows the current-voltage (*I-V*) characteristics of a poly-Si diode without phase change layer. The device size is 150 × 150 nm. In the range of $V > 0.9$ V, *I-V* is measured by pulse test (t_w = 100 ns) to avoid excessive stress. The forward current density at 1.5 V was ~ 13 MA/cm^2 and the reverse current at -2.0 V was ~ 1 A/cm^2. Extrapolated off leak current at 100°C is less than 10 A/cm^2 (Fig. 5). To investigate the endurance of the diode against repeated stress pulses, reverse leak currents after stress pulses were measured (Fig. 6). In applying 13-MA/cm^2 stress pulses, off-leak exceeded 10 A/cm^2 after 10^5 repeated times. In the case of 11-MA/cm^2 stresses, on-off ratios remained higher than 6 orders of magnitude after 10^6 repeated times.

Next, the characteristics of the 1D1R devices with phase change layer are shown. The resistance change as a function of programming currents is plotted in Fig. 7. The device size is 100 × 100 nm. Read current was extracted from the value at 1.0 V in the *I-V* curves shown in Fig. 8. Current density required for reset programming was 11.5 MA/cm^2. This value is larger than our previous work [3] possibly because of the difference of the sputtering machine. Reset current was almost proportional to the device size (Fig. 9). Reset current of GST measured as 25 MA/cm^2 in the slimmed-GST structure (the top metal/GST line is 80 nm in width and the diode under GST is 200 × 200 nm), since the reset current of GST was quite higher than drivability of the diode. Selected reset/set programming of four cells with no disturbance was confirmed in a 16 × 16 array of 100-nm half pitch (Fig. 10). We also estimated thermal disturb in a finer pitch array. The temperature distribution during reset pulse was simulated in the 50-nm half pitch (Fig. 11). Calculated temperature of the neighboring cell was lower than 200°C, which is below the crystallization temperature.

4. Summary

The phase change memory of cross-point array structure is fabricated. We have shown performances of drivable unipolar diode and low-power nano-GST and demonstrated selective reset/set programming in the 4F^2 array.

Acknowledgements

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References

[1] Y. Sasago *et al*., Symp. VLSI Tech. 2009, pp. 24-25.
[2] S. H. Lee *et al*., Tech. Dig. IEDM 2011, s3p3.1-4.
[3] T. Morikawa *et al.*, Tech. Dig. IEDM 2012, s31p4.1-4.
[4] The 3rd Report on Ultra Low Voltage Device Project for Low-Carbon Society (in Japanese), January 2014.

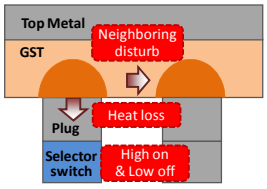

Fig. 1 Issues of cross-point memory cell.

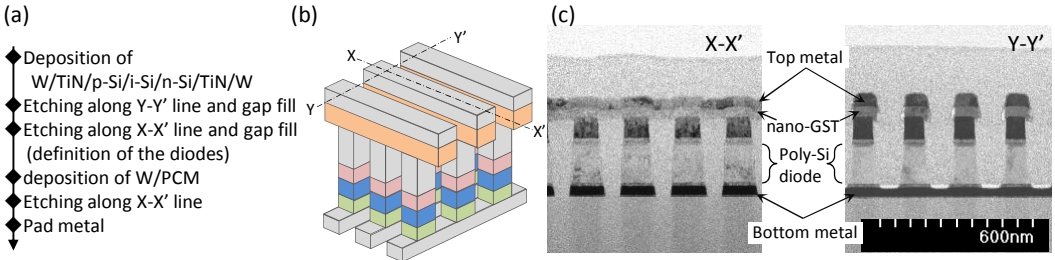

Fig. 2 Cross-point phase change memory.(a) process flow of our phase change memory, (b) birds' eye schematic of the fabricated structure, (c) TEM images of X-X' and Y-Y' cross sections.

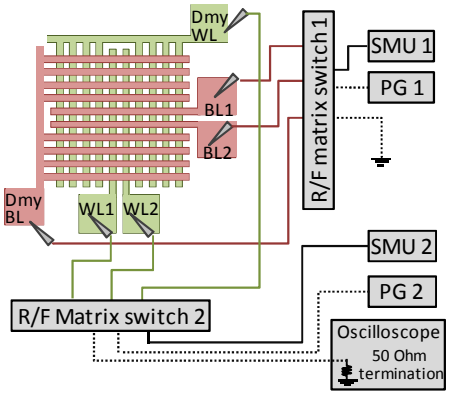

Fig. 3 Top-view layout of the fabricated cross-point test structure and measurement setup.

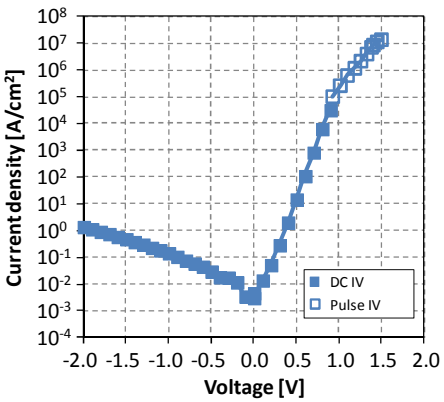

Fig. 4 Current-voltage characteristics of a poly-Si diode. The size is 150 x 150 nm.

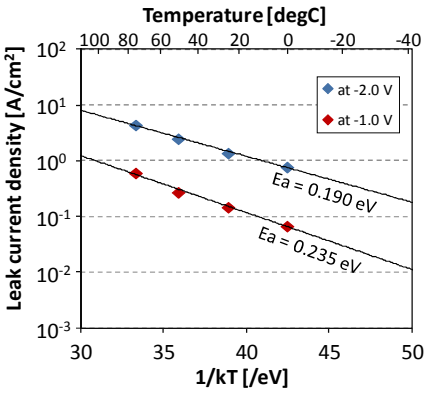

Fig. 5 Temperature dependence of off current of a poly-Si diode.

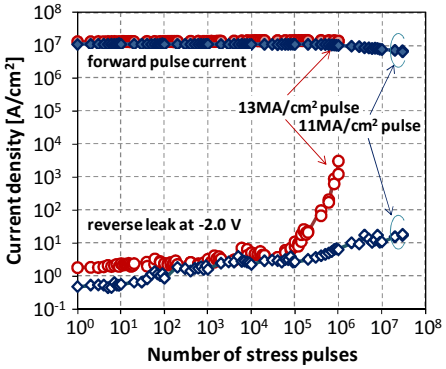

Fig. 6 Endurance characteristics of a diode against repeated stress pulses.

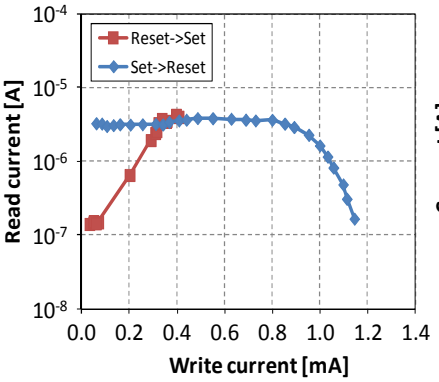

Fig. 7 Programming characteristics of a 1D1R cell. The size is 100 x 100 nm.

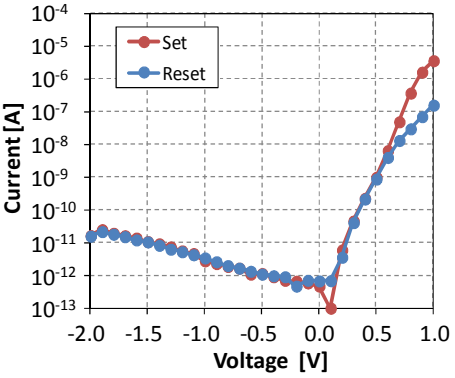

Fig. 8 Current-voltage curves of a 1D1R cell in reset and set states.

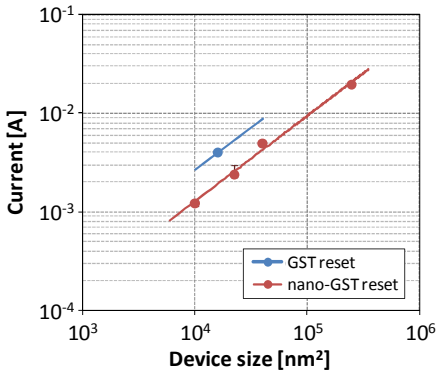

Fig. 9 Dependence of reset currents of GST and nano-GST on device size.

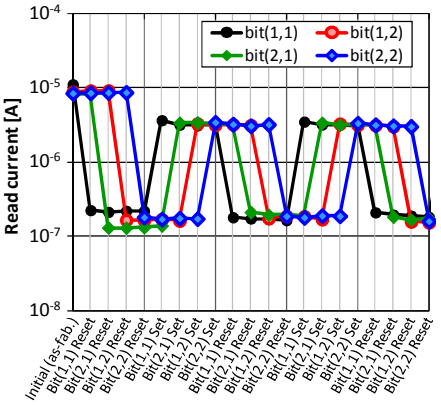

Fig. 10 Selective reset/set switching without no disturb. The test array is 16 x 16 and half pitch is 100 nm.

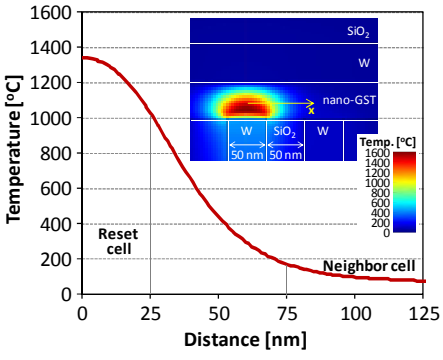

Fig. 11 Calculated temperature distribution of the array (F = 50 nm) during applying reset pulse (t_w = 20 ns).