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Properties of Perpendicular-Anisotropy Magnetic Tunnel Junctions Fabricated over The Cu Via

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Abstract

We have fabricated perpendicular-anisotropy magnetic tunnel junctions (MTJs) over Cu vias on 300 mm wafers and measured their magnetoresistance properties. MTJs prepared on the polished metal over the Cu via exhibited no electrical short, high median value of normalized MR ratio and low standard deviation value of MR ratio. These results suggest that the surface of the polished metal was smooth. This technology contributes to the small memory cell size of spin transfer torque magnetic random access memory (STT-MRAM).

1. Introduction

Applications that use magnetic tunnel junctions (MTJs) such as spin transfer torque magnetic random access memory (STT-MRAM) and nonvolatile logic-in-memory architecture have been attracting much interest [1-3]. To achieve such practical applications, MTJs need to satisfy high tunnel magnetoresistance (TMR) ratio, low switching current and high thermal stability factor.

We have successfully demonstrated that CoFeB/MgO based MTJs with a perpendicular anisotropy has potential to satisfy these requirements at the same time [4]. Moreover, high density STT-RAM requires the small memory cell size. To achieve the small memory cell size, it is beneficial to prepare the MTJ over the Cu via. In this paper, perpendicular-anisotropy MTJs (p-MTJs) were prepared on three types of substrates. First, MTJs were prepared on the SiO_2 substrate. Secondly, MTJs were located directly on the Cu vias. Finally, MTJs were fabricated on a polished metal over the Cu vias. In this paper, we have prepared the MTJs of these structures on 300 mm wafers and reported their magnetoresistance properties.

2. Experimental

All the stack structures in this study were prepared by sputtering at room temperature on 300 mm wafers. The MTJ structures consisted of, from the substrate side, bottom electrode / [Co/Pt] multilayer / Ta / CoFeB / MgO / CoFeB / Ta / Ru / Ta top electrode. The resistance-area product RA of the MTJs was 12 $\Omega\mu m^2$. The samples were annealed at 300℃ for 1 h.

Figure 1 shows a schematic process flow for forming an MTJ structure. An MTJ stack including a metal hard mask was deposited on the copper wired substrate (1(b)). A metal hard mask was formed with an insulating hard mask. Using the metal hard mask, an MTJ was etched to a bottom electrode layer (1(c)). Next bottom electrode was formed using the insulating hard mask. After interlayer dielectrics deposition, planarization process was performed (1(d)). The insulating film on top of MTJs was etched-back, stopping the top metal hard mask. This process opened the top contact of the junction for an upper electrode. Finally, the upper electrode was formed (1(e)). The size of the MTJs was 80 nm.

The MTJs were fabricated on three kinds of substrate geometries, as shown in Fig. 2. In Fig. 2(a), the MTJ was fabricated on the SiO_2 insulating film. We named the MTJ geometry an off-axis geometry. In Fig. 2(b), the MTJ was prepared directly on the Cu via. We named the MTJ geometry direct on-axis geometry. The size of the Cu via was 140 nm

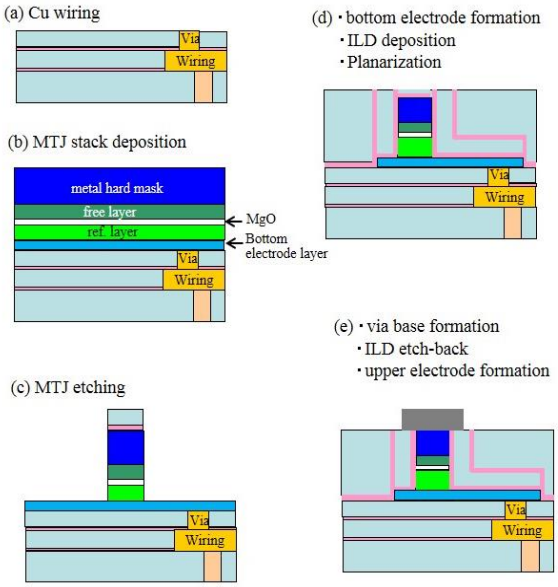

Fig. 1 Process flow for forming an MTJ structure.

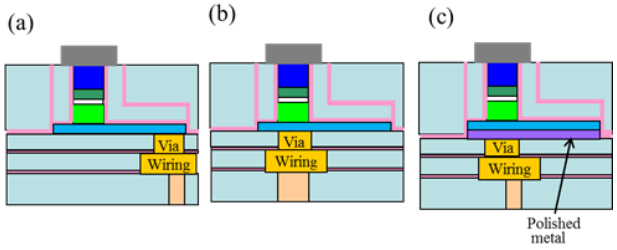

Fig. 2 MTJs were fabricated on three kinds of substrate geometry. (a) The MTJ onto the SiO_2 insulating film, (b) the MTJ directly on the Cu via and (c) the MTJ on the polished metal layer over the Cu via.

in diameter. Moreover, MTJs were prepared on the polished metal layer over the Cu vias. Fabrication process of the MTJs on the polished metal layer was as follows. The metal layer was deposited on the substrate with Cu vias. The surface of the metal layer was polished mechanochemically. The MTJ stack structures were deposited on the polished metal layers and patterned into junctions, described above. We named the MTJ geometry polish on-axis geometry.

Magnetoresistance properties of the MTJs were measured at constant voltage of 10 mV. Applied magnetic field ranged from -1250 Oe to 1250 Oe with 25 Oe step. A 300 mm wafer contained 80 chips. We measured one typical MTJ per one chip. Total 80 MTJs were measured in the whole 300 mm wafer.

Figure 3 shows cumulative probability of normalized MR ratios for MTJs with the three geometry. MR ratios were normalized by maximum MR ratio with off-axis geometry. Figure 3(a) exhibits the properties with off-axis geometry. There were no electrical short nor open devices. Median value of normalized MR ratio was 0.916. Standard deviation of normalized MR ratio was 3.4 %. Figure 3(b) exhibits cumulative probability of normalized MR ratios with direct on axis geometry. 6 MTJs showed normalized MR ratio below 0.8, indicating 6 MTJs were electrically short. Standard deviation of normalized MR ratios over 0.8 was 5.4 %. This value was larger than 3.4 % for MTJs with off-axis geometry, suggesting that electrical weak short occurred for MTJs with direct on axis geometry. This effect was explained as a roughness of the Cu via surface. The median value of normalized MR ratio was 0.871, which was lower than 0.916 with off-axis geometry.

Figure 3(c) presents cumulative probability of normalized MR ratios with polish on-axis geometry. Median value of normalized MR ratios was 0.928, which was higher than 0.916 with off-axis geometry. Median value of R_{min} for MTJs with polish on-axis geometry was 2650 Ω, whereas median value of R_{min} for MTJs with off-axis geometry was 2700 Ω. The R_{min} difference was originated from the bottom electrode resistance between the MTJ and the Cu via. The elimination of the bottom electrode resistance with polish on-axis geometry caused higher normalized MR ratios. Standard deviation of normalized MR ratio was 3.0 %, which was lower than 3.4 % with off-axis geometry. It seems that the surface of the polished metal was smoother than the SiO_2 surface under MTJs with off-axis geometry. Further study of structural characterization is now in progress.

3. Conclusions

We have prepared p-MTJs on 300 mm wafers. These MTJs were fabricated on three types of substrates and magnetoresistance properties were measured. MTJs located directly on the Cu vias showed electrical short and low median value of MR ratio. On the contrary, MTJs prepared on the polished metal over the Cu vias exhibited no electrical short, high median value of MR ratio and low standard deviation value of MR ratio. These results suggest that the surface of the polished metal was smooth. This technology contributes to the small memory cell size of STT-MRAM.

Acknowledgements

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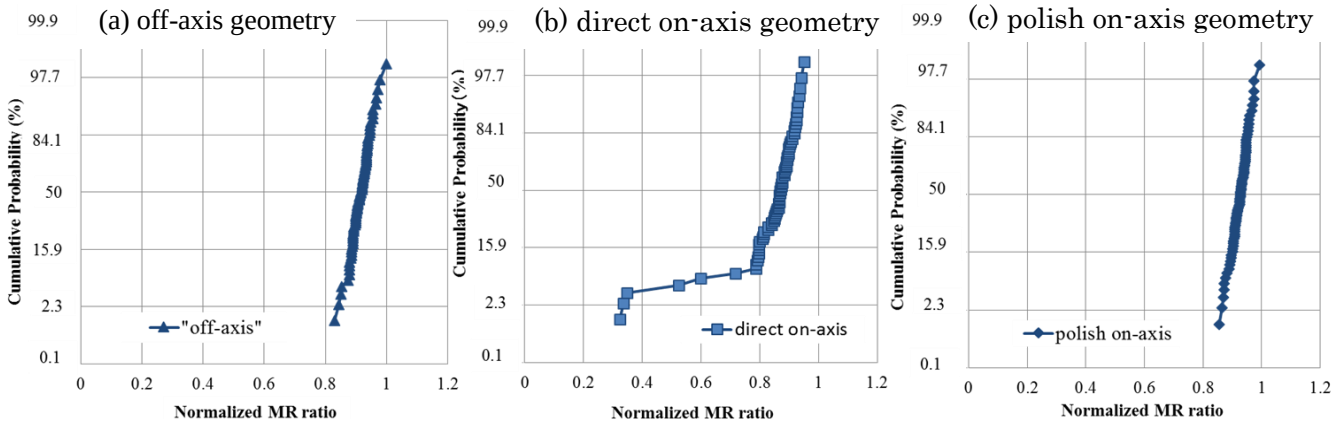

Fig. 3 Cumulative probability of normalized MR ratios for MTJs (a) with off-axis geometry, (b) with direct on-axis geometry and (c) with polish on-axis geometry. MR ratios were normalized by maximum MR ratio with off-axis geometry.