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CAAC-OS-based Nonvolatile Programmable Analog Device: Voltage Controlled Oscillator Realizing Instant Frequency Switching

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Abstract

A VCO using programmable analog memory (PAM) as a voltage-controlled element is developed as a programmable analog device including a c-axis aligned crystalline In-Ga-Zn oxide FET. The oscillation frequency of the VCO is controlled by analog voltage data (AVD) stored at the PAM. The frequency can change over six orders of magnitude with a driving voltage of 1.5 V and AVD ranging from 0.7 to 2.5 V. This is realized by switching among PAMs that keep their values with infrequent AVD refresh. A low-power PLL using the VCO is also proposed.

1. Introduction

A c-axis aligned crystalline In-Ga-Zn oxide (CAAC-IGZO), a crystalline oxide semiconductor (OS), can be used to achieve a FET exhibiting ultra-low off-state current [1]. LSI [2]–[7] as well as display [8] applications utilizing the CAAC-IGZO FET have been developed. They include field-programmable gate arrays (FPGAs), having CAAC-IGZO FET-based nonvolatile configuration memory [5]–[7], that employ a multi-context architecture to realize instant configuration switching and require extremely low power for data retention.

The CAAC-IGZO FET-based configuration memory in these FPGAs works as memory holding binary digital data; it also has the potential to work as nonvolatile programmable analog memory (PAM) that can keep the values.

As an example application of a programmable analog device, this paper reports on a VCO using nonvolatile PAM with a CAAC-IGZO FET as a voltage-controlled element (VCE). The VCO outputs a signal with intended oscillation frequency in accordance with analog voltage data (AVD) stored at PAM and is capable of switching frequencies at high speed and obtaining stable oscillation in a short time after power-on.

2. Design and Fabrication

Fig. 1 is a circuit diagram of the fabricated VCO. The VCO is a ring oscillator composed of 101-stage inverters and voltage-controlled switches (VCS) between the inverters. Each VCS consists of multiple VCEs (VCE[i]). VCE[i] stores intended AVD (V_{DATA}) at a node SN, and the channel resistance of a transistor MG is controlled based on the AVD when the AVD is well controlled by a circuit for setting voltage. In other words, the VCS resistance is based on the AVD programmed in a selected VCE to enable control of the VCO oscillation frequency. With the use of a CAAC-IGZO FET as a transistor MW, the node SN is regarded as floating when the transistor MW is off; thus, the AVD can be kept for a long time.

Multiple VCEs have the following advantage: by programming different AVD in the VCEs and changing selection of VCEs, the oscillation frequency of the VCO can be switched immediately in accordance with AVD programmed in the selected VCE.

The VCO has been fabricated with a hybrid process involving a 1.0 μm CAAC-IGZO FET and a 0.5 μm CMOS FET [2]–[7]. Fig. 2 shows the static characteristics of a CAAC-IGZO FET. The off-state current of this FET is extremely low; an off-state current of a CAAC-IGZO FET with a channel length of 3 μm is approximately 5E−23 A/μm at 85 °C [9].

3. Measurements and Results

3-1. Oscillation Frequency vs. V_{DATA}

Fig. 3 shows the relationship between oscillation frequency and AVD programmed in each VCE; the relationship is measured on a test element group with a VCS having four VCEs. The driving voltage V_{RO} of the inverter is 1.0, 1.5, or 2.5 V. The driving voltage V_{CL} of a circuit selecting the gate of the transistor MW is 2.5 V. The backgate voltage V_{BG} of the transistor MW is −9.0 V. The write time is 500 μs.

The results of selecting only VCE[1] show the VCO oscillation frequency depends on the level of V_{DATA}. For example, at V_{RO} of 1.5 V, the oscillation frequencies are 7.20 Hz and 7.83 MHz with V_{DATA} of 0.7 V and 2.5 V, respectively. In other words, the VCO changes the oscillation frequency over six orders of magnitude with V_{RO} ranging from 0.7 to 2.5 V. Note that inverter delay may be dominant in a region with high V_{DATA}; therefore, the oscillation frequency does not depend significantly on V_{DATA}. On the other hand, in a region with low V_{DATA}, specifically 1.3 V or lower, oscillation frequency depends strongly on V_{DATA}.

With regard to oscillation frequency dependence on V_{RO}, with V_{RO} of 1.0 and 2.5 V, the highest oscillation frequencies are 2.30 and 9.09 MHz, respectively, and the maximum gradients of the log-scale oscillation frequency with respect to V_{DATA} are 0.47 and 1.08 decades per 100 mV, respectively. Accordingly, V_{RO} may be changed to meet intended applications of the VCO; for example, a high driving voltage is used to obtain a wide frequency range, and a low driving voltage is used to control the frequency at short intervals.

3-2. Oscillation Frequency Retention

Fig. 4 shows frequency retention characteristics, i.e., oscillation frequency spectra of the VCO and the change with time when V_{DATA} is 1.5 or 2.5 V. In the initial state, power consumption of the VCO with V_{DATA} of 2.5 and 1.5 V is 795 and 336 μW, respectively, and figures of merit [10] are estimated at −127.7 and −134.3 dBc/Hz.

With V_{DATA} of 2.5 V, the central oscillation frequency is decreased by 1.2% in 90 min. In contrast, with V_{DATA} of 1.5 V, the central oscillation frequency is attenuated by 4.0% in 5 min. This probably occurs because the rate of increase of the oscillation frequency to V_{DATA} is higher at V_{DATA} of approximately 1.5 V than when it is approximately 2.5 V, and thus a small fluctuation of AVD programmed in a VCE greatly influences the oscillation frequency.

The results demonstrate that the oscillation frequency of the VCO can be kept constant by re-programming AVD with refresh at very long intervals. Depending on the AVD, changing the interval between refreshes is effective.

3-3. Frequency Switching

Owing to nonvolatile analog memory, the VCO is capable of maintaining the oscillation frequency after power-off and subsequent reboot. Fig. 5 shows the waveform of an output OUT of the VCO when the VCO in the off state is rebooted with V_{DATA} of 2.5 V. Fig. 5 demonstrates that when power supply is restarted at time (α + 1.0) μs, oscillation is restarted in less than 30 ns.

Furthermore, programming different AVD in VCEs of the VCO enables instant switching of the oscillation frequency. Fig. 6 shows the oscillation frequency is switched by changing selected VCE between VCE[1] and VCE[2] when V_{RO} is 1.5 V. It is clear from Fig. 6 that the frequency is switched in less than 100 ns.

4. PLL Application

In a general PLL, circuits other than a VCO are forced to operate even after oscillation of the VCO is stabilized. These circuits account for a large proportion of the total power consumption. It has been reported that in a PLL operating at approximately 20 GHz and 1.5 V, circuits other than the VCO account for 60% of the total current consumption [11].

In contrast, in a PLL including the proposed VCO, circuits excluding the VCO can be powered off in periods other than an infrequent refresh period required to maintain the oscillation frequency; thus, power consumption can be drastically reduced. Further, in rebooting the PLL, AVD corresponding to the previous oscillation frequency can be held, which should result in high-speed rebooting.

References

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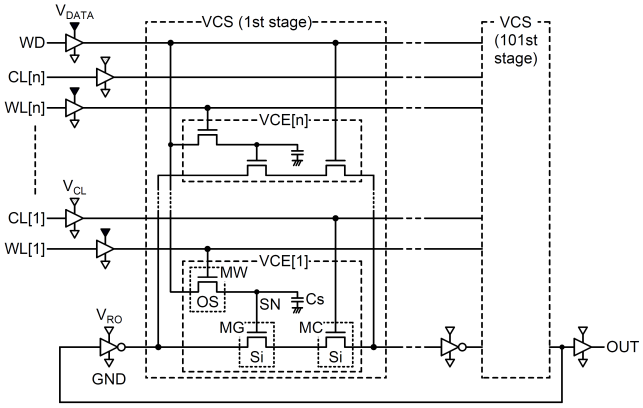

Fig. 1 Circuit diagram of proposed VCO including CAAC-IGZO FET with channel width $W = 4$ μm and Si FET with $W = 16$ μm

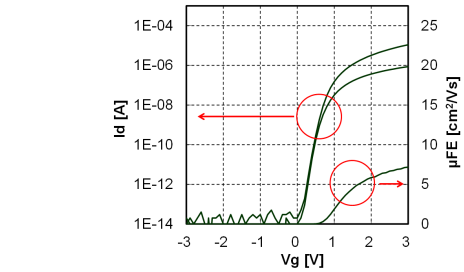

Fig. 2 Characteristics of CAAC-IGZO FET

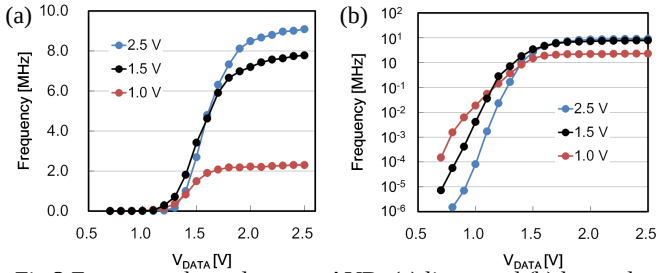

Fig.3 Frequency dependence on AVD; (a) linear and (b) log scales

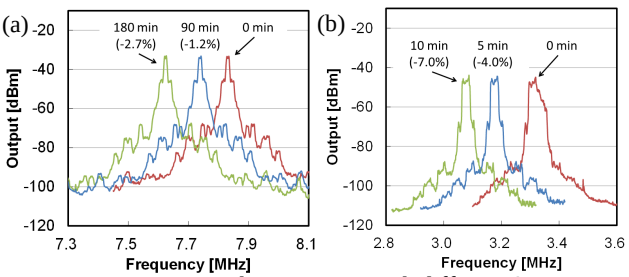

Fig. 4 Data retention characteristics with different AVD (V_{RO} = 1.5 V); (a) V_{DATA} = 2.5 V, (b) V_{DATA} =1.5 V

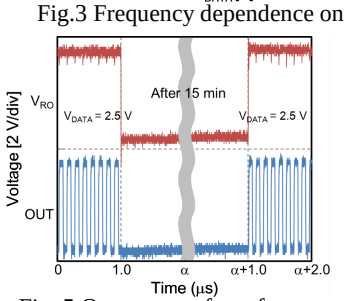

Fig. 5 Output waveform from power-off to reboot; α = 15 min

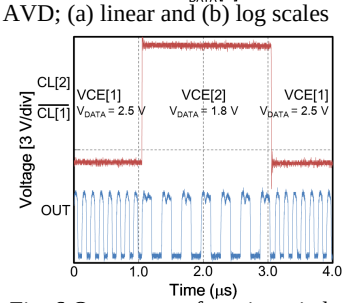

Fig. 6 Output waveform in switching selected VCE; V_{RO} = 1.5 V