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A 500ps/8.5ns Array Read/Write Latency 1Mb Twin 1T1MTJ STT-MRAM designed in 90nm CMOS/40nm MTJ Process with Novel Positive Feedback S/A Circuit

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Abstract

A positive feedback S/A is proposed that can achieve 500ps array read latency for 1Mb twin 1T1MTJ STT-MRAM designed in 90nm CMOS/40nm MTJ under 8.5ns write latency. This S/A also relaxes the requirement on MTJ's thermal stability factor $\Delta=E/k_bT$ to 'Δ>70' from 'Δ>90' in the conventional S/A estimated with the condition of 1FIT error rate in 10 years for 256Mb array with the same design rule.

1. Introduction

Static power increase in cache memories is one of the bottlenecks in improving computer performance. It is expected that high-performance nonvolatile (NV) memories using spin-transfer-torque magnetic tunnel junctions (STT-MTJs) will be applied to the cache to reduce the static power drastically. There have been proposed several differential pair type STT-MRAM cells for performance-oriented applications [1]-[3]. However, their sizes are large for the high-density applications. A smaller twin 1T1MTJ cell was proposed [4]. However, the access time (4ns) is not fast enough. In this paper, we propose a S/A with positive feedback loop to latch the sensing nodes very fast. This scheme also provides substantially read disturb-free data sensing.

2. Cell and S/A Design

Fig.1 shows the proposed S/A scheme compared with the conventional one [5] for twin 1T1MTJ cell. The conventional sensing scheme relies on a differential amplifier such as a current mirror type, the sensing of which is rather slow. On the other hand, the proposed S/A can latch a pair of sensing nodes very fast, because the sensing is performed in a positive feedback loop that is formed in the current path.

Fig. 2 is the actual implementation of the cell and the S/A into the 2kb unit (256 rows by 8 columns). A S/A and a DQ buffer (DQB) are shared among eight columns. The unit is repeated 16 times in the row direction to make a 64kb cell array. Fig. 3 shows a 1Mb twin 1T1MTJ STT-MRAM macro consisting of sixteen 64kb cell arrays.

Fig. 4 shows the array read latency simulated for the 1Mb twin 1T1MTJ STT-MRAM with the proposed positive feedback S/A that is compared with the conventional current mirror S/A. The signal development times in which the voltage difference between a pair of bit lines (BL and BBL) is amplified to 80mV are compared. The proposed S/A can develop the signal in 500ps, while the conventional S/A takes 2.1ns for the signal amplification. Thus the positive feedback sensing scheme is shown to be effective in high-speed signal sensing for twin 1T1MTJ STT-MRAM.

The scaling trend of MTJ switching time in the twin 1T1MTJ cell is shown in Fig. 5. In the simulations, the channel width and the gate length of the PFET selective device is kept constant at 0.64μm and 0.1μm, respectively. The cell can be switched in 8.5ns for 40nm size MTJ.

3. Read Disturb Failure Rate

Fig. 6 shows the simulated currents flowing through a pair of MTJs in a cell for the both sensing schemes. It is shown that the disturb current is suddenly attenuated due to the positive feedback loop in the proposed S/A, while the read disturb current continues to flow in the conventional sensing scheme. The read disturb-failure rate of 256Mb twin 1T1MTJ STT-MRAM with 512b parallel read using the proposed sensing scheme is shown in Fig. 7 as a function of the MTJ's energy barrier normalized by thermal energy E/k_bT compared with the retention-failure rate. The read disturb-failure rate is shown smaller than the retention-failure rate. On the other hand, the failure of the STT-MRAM with the conventional S/A is limited by read disturb and 'E/k_bT > 90' is required for realizing the macro whose failure rate is less than a few FIT. By adopting the proposed S/A, the required energy barrier is limited by retention and relaxed to 'E/k_bT > 70', which falls within a realizable range [6].

The 512b parallel write current of 256Mb twin 1T1MTJ STT-MRAM using the architecture was simulated to compare with 6TSRAMs as shown in Table I. It is much smaller than low operating power (LOP) SRAM and even smaller than low standby power (LSTP) one, due to the elimination of static current in cells.

4. Chip Features

Fig.8 shows the microphotograph of the 1Mb twin 1T1MTJ STT-MRAM measuring 1.4mm^2, being 59% reduction from the 4T2MTJ counterpart [3] due to the cell size reduction and the elimination of PL drivers used for the power gating in the 4T2MTJ STT-MRAM. Fig. 9 is the operational waveforms of the chip. Table II summarizes the features of the 1Mb twin 1T1MTJ STT-MRAM.

Acknowledgments

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References

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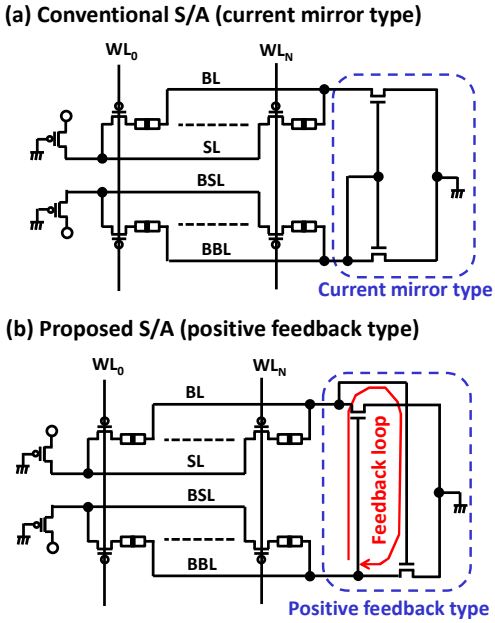

Fig.1 The conventional S/A (a) and the proposed one (b) for twin 1T1MTJ cell.

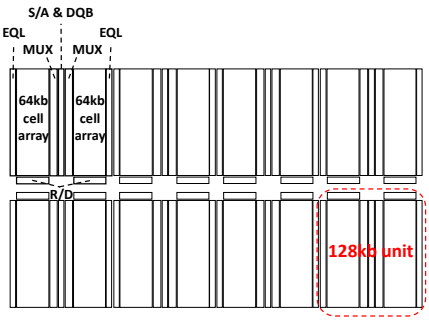

Fig.3 1Mb twin 1T1MTJ STT-MRAM macro using the 2kb unit in Fig. 2.

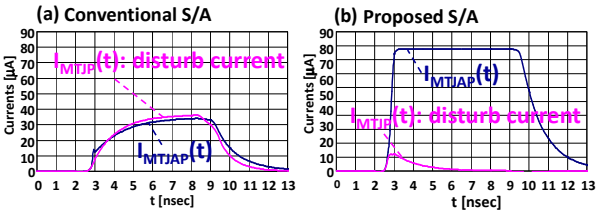

Fig.6 Simulated currents through MTJs for the conventional S/A and the proposed S/A. The current flowing through the parallel MTJ I_{MTJP} causes the MTJ to be switched during read (read disturb).

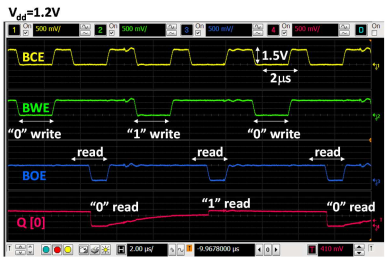

Fig.9 Measured operational waveform of 1Mb twin 1T1MTJ STT-MRAM.

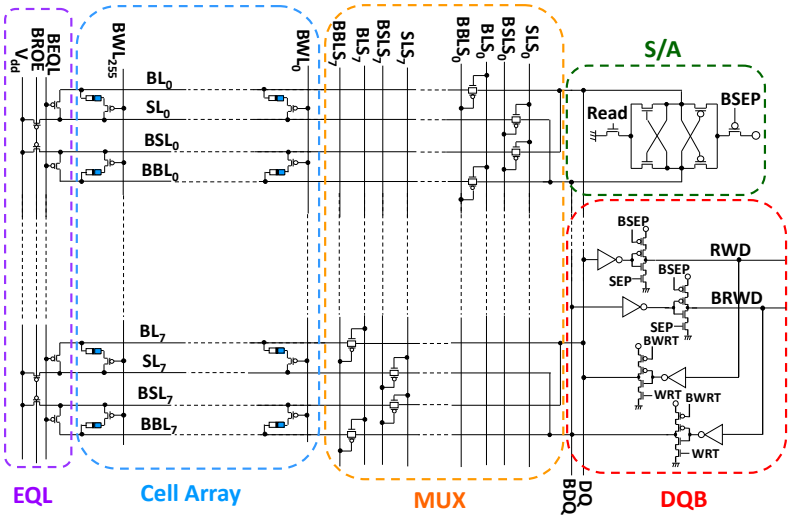

Fig.2 2kb unit of 1Mb twin 1T1MTJ STT-MRAM using the proposed positive feedback S/A.

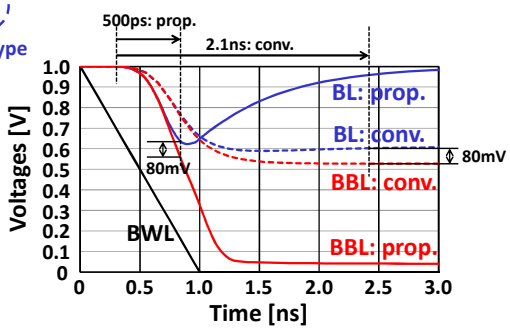

Fig.4 Array read latency of the proposed S/A under the same condition as the conventional one.

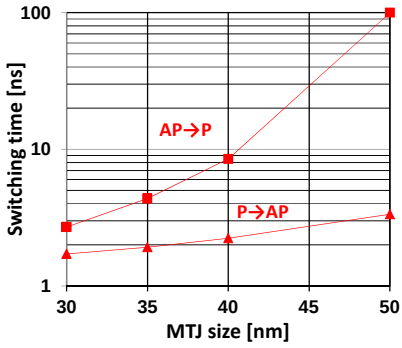

Fig.5 Scaling trend of MTJ switching time for the 1T1MTJ cell (PFET selective device size is unchanged at W/L_g= 0.64μm/0.1μm). P and AP stand for parallel state and anti-parallel state, respectively.

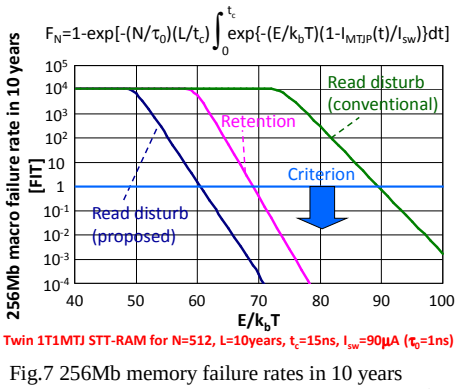

Fig.7 256Mb memory failure rates in 10 years use. The parameters shown at the bottom of the graph are used to calculate the failure rates by the equation at the top of the graph.

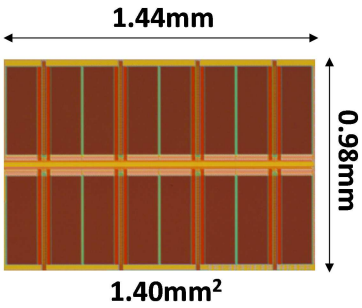

Fig.8 Photograph of fabricated 1Mb twin 1T1MTJ STT-MRAM macro.

Table I 512b write current of 256Mb twin 1T1MTJ STT-MRAM compared with 6T SRAMs.

		Twin 1T1MTJ STT-MRAM	6TSRAM	
			LOP	LSTP
Power supply voltage		0.9 V	0.9V	
Total Current/256Mbit (Write cycle @15ns)		**77mA**	**1.46A**	**138mA**
Components	Write Current/512bit	70mA	0.18mA	
	Write Current/cell	136μA	0.36 μA	
	Array Control Current/512bit	7mA	4mA	
	Static Current/256Mbit	0	1.46A	134mA

Table II Features of 1Mb twin 1T1MT STT-MRAM.

	1Mb twin 1T1MTJ STT-MRAM
Process	90nm CMOS (Lg=100nm) + MTJ
Cell size	0.88μm^2
Macro size	1.40mm^2/1Mb
Cell efficiency	66%
Supply voltage	1.0V
Organization	64k word x 16bit
Access time	400ps (V_{dd}=1.0V,RT)
Read current	52mA (V_{dd}=1.0V, 2ns cycle)
Write current	23mA (V_{dd}=1.0V, 5ns cycle)