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Trends on Advanced Semiconductor Memories

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Abstract

This talk will review the history, in which memories have overcome the scaling issues, and then look toward future, which are market trends, technical issues and actions of future advanced memories. As promising solutions to break through the scaling limitation for the future advanced memories, I will discuss the Bit Cost Scalable (BiCS) technology, which enormously reduces the bit costs by vertically stacking memory arrays with stack, punch and plug process, and 3D chip stacking technology, which introduces new features.

1. Introduction

The semiconductor memories have amazingly evolved for 40 years and more, based on DRAM technology and scaling law, which Dr. R. H. Dennard invented and proposed [1]. Now, 28nm technology node DRAM's are mass-produced, which has 360x reduction of feature size, and around 6 order reduction of cell size with advanced lithography, capacitor, and transistor technologies etc.. On the other hand, NAND flash has scaled down more rapidly for around 20 years. The feature size has reduced from 350nm to 19nm, reduced by 18x for 17 years. The cell size has reduced by 2000x, introducing new technologies, such as self-aligned STI, multi-level cell operation, and so on.

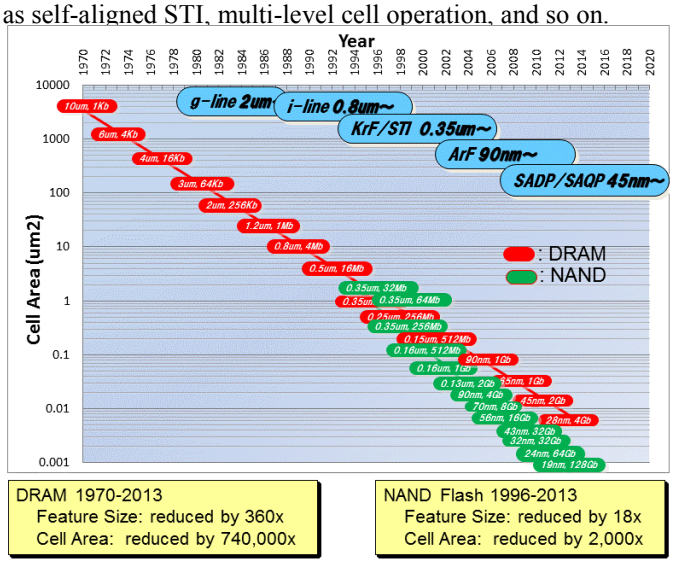


Fig. 1 Scaling history of DRAM and NAND flash.

2. Trends of markets and technologies

In the DRAM market trends, recently, there are market diversifications to meet customer's needs, such as low power for mobiles, high speed and high reliability for sever, networking, and graphics applications. According to market research, there will be data big bang of data created by human being and machines in future. In 2013, it was 5 zeta byte. It will be 20 zeta byte in 2018 and 40 zeta byte in 2020. Many cloud service providers are aiming at new business to analyze big data and provide new services. According to this trend, the market of data storage memory will continue to rapidly expand. We've expanded NAND applications using bit price reduction. With much more bit price reduction, NAND markets will continue to expand. The other application markets are storage class memory (SCM) markets, which can fill the gap between DRAM and NAND flash to enhance the performance of memory systems.

Figure 2 shows the positioning of various memories, which is the relationship, write or program cycle time vs. the bit capacity. There are three categories in memory positioning, which are working memory, code storage memory or SCM, and data storage memory. In the working memories, MRAM is a promising memory to overcome DRAM with relatively high speed and medium bit capacity. In the code storage memories, PRAM is a representative memory to replace NOR flash and create SCM application field. In the data storage memories, 3D-NAND or BiCS-type nonvolatile memories can supply extremely high density with high data rates to extend data storage application.

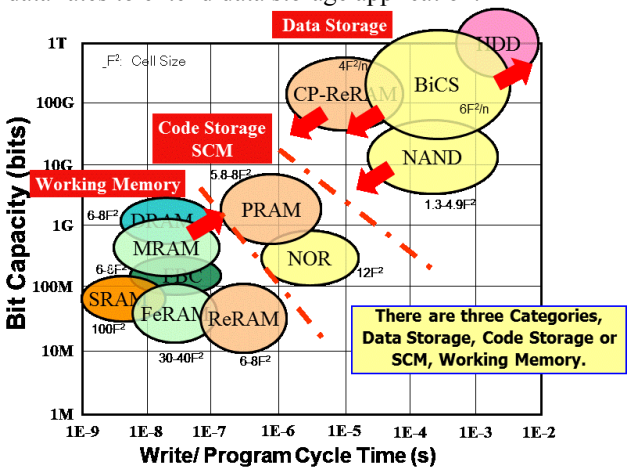


Fig. 2 Positioning and forecast of various memories.

3. BiCS technology

We proposed the BiCS technology [2,3], which stacks multilayer of plate electrodes and dielectric films, punches the whole multilayer stack from top to bottom only by one critical hole lithography and one etching process, and plugs

the inside of holes with the memory film and pillar electrodes. Memory cells are located at the intersections of plate electrodes and pillar electrodes. BiCS process leads to extremely drastic and continuous bit cost reduction, compared with simply stacked array structure and cross point array structure.

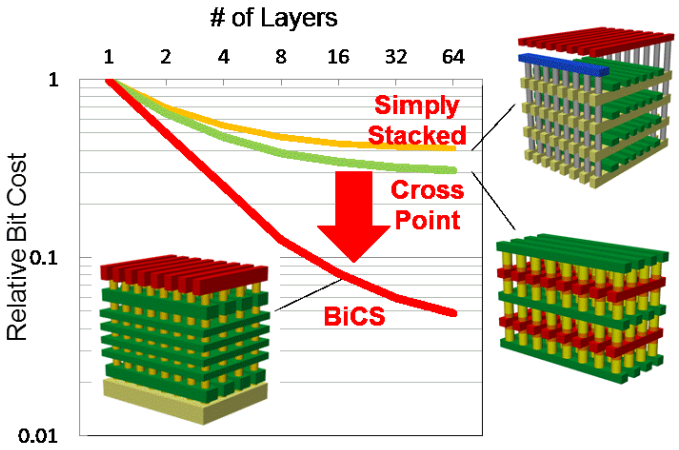


Fig. 3 Comparison of bit cost among 3D memories.

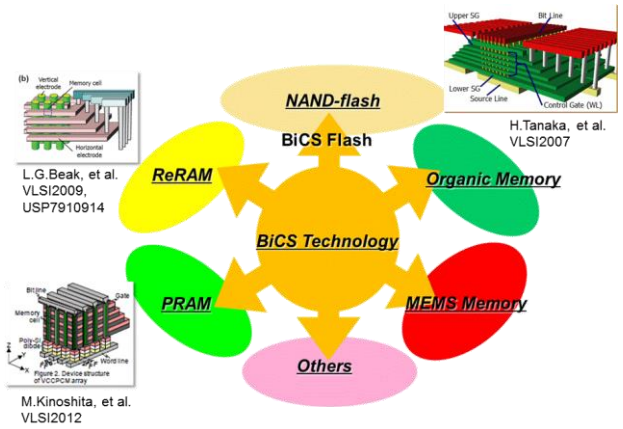


Fig. 4 Expansion of BiCS technology into various memories.

We can apply the BiCS concept to various memories. Recently, ReRAM and PRAM with BiCS-type array structures were reported to meet bit cost requirements of high density applications [4-6].

4. 3D chip stacking technology

There are two ways of 3D IC, which are 3D Process Integration, and 3D Chip Stacking. 3D Process Integration is very much suitable for low cost and high density memories. We've proposed BiCS technology to get extremely low bit cost and super high density flash or nonvolatile memories to break through the scaling limitations of 2D devices. On the other hand, 3D chip stacking is suitable for small form factor, high speed, low power, and multi-functionality. Introducing Through-Silicon-Via, TSV, we can accelerate the advantages to get higher bandwidth, higher density, lower power memories or logic and memory stack solutions. High bandwidth, high density and high speed flash or DRAM 3D chip stacking products have been proposed.

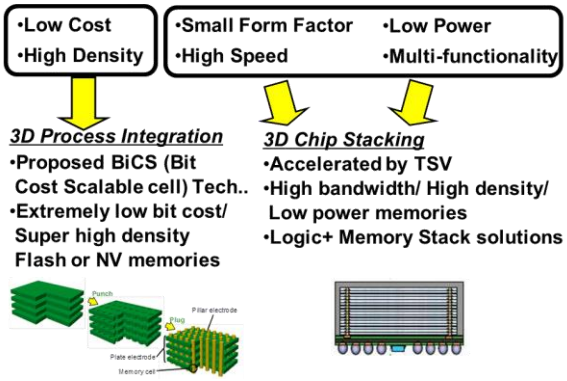
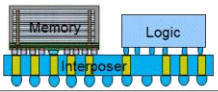


Fig. 5 Two ways of 3D IC, which are 3D Process Integration, and 3D Chip Stacking.

Table 1 Comparison between 2.5D IC and 3D IC.

	2.5D IC	3D IC
Structure		
Advantages	-Thick & existing chips available -Easy pad design matching b/w chips -Easier heat release	-Higher data rate -Smaller PKG size -Lower power
Disadvantages	-Lower data rate -Larger PKG size	-Need chip thinning -Harder pad design matching b/w chips -Harder heat release
Applications	-High density FPGA -Integration of heterogeneous chips	-LP & high speed NAND -Hybrid Memory Cube (HMC) -Mobile processor w/ wide I/O DRAM etc.

2.5D IC has advantages, so that thick and existing chips, easy pad design matching between chips, and easy heat release are available. But, it has lower data rate and larger package size. On the 1st stage of market introduction, 2.5D IC is more suitable for mass productions. 3D IC has disadvantages such as chip thinning, harder pad design matching between chips, and so on. But it is able to realize much higher data rate, smaller package size and lower power.

5. Conclusions

I reviewed amazing scaling of advanced memories, and forecasted the trends of markets and technologies. BiCS technology has the large potential for future high density data storage memories to overcome 2D scaling limitation. BiCS flash is the most promising candidate as super high density storage device to achieve terabit generation. 3D chip stacking is helpful for higher performance and multi-functionality.

Acknowledgements

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References

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