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# Substrate Doping Concentration Dependence on Random Telegraph Noise Spatial and Statistical Distribution in 30nm NAND Flash Memory

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## Abstract

The dependence of the spatial and statistical distribution of random telegraph noise (RTN) in a 30nm node NAND flash memory on substrate doping concentration $N_A$ are comprehensively investigated using 3-D Monte Carlo device simulation. Since $N_A$ in NAND flash memory is relatively low to suppress junction leakage current during channel boost operation, it is found that RTN amplitude $\Delta V_{th}$ is larger at the center of the channel region, which is closer to the jellium doping results. In such case, $\Delta V_{th}$ distribution slope $\lambda$ cannot be determined by only considering random dopant fluctuation (RDF).

## Introduction

RTN is considered to be one of the main noise/error sources in ultra-scaled NAND flash memory technology. The distribution of the single-trap RTN amplitude represented by the threshold voltage shift $\Delta V_{th}$ (Fig. 1) in the NOR flash memory cells has been intensively investigated using 3-D device simulation that features RDF [1-3]. In these reports, $\Delta V_{th}$ shows exponential distribution $\lambda$ with a standard deviation proportional to the square root of the $N_A$ assuming uniform doping profile with relatively high $N_A$ region beyond $1\times10^{18}$cm$^{-3}$. Meanwhile, in NAND flash memory, $N_A$ is expected to be kept as low (< $1\times10^{18}$cm$^{-3}$) as possible to suppress junction leakage current and maintain sufficiently high channel voltage (~8V) during program inhibit operation as shown in Fig. 2 [4]. In this work, $N_A$ is widely varied and the $\Delta V_{th}$ spatial and statistical distribution is comprehensively investigated using 3-D Monte Carlo device simulation considering RDF in 30nm node aiming NAND technology (Table I). Uniform jellium doping cases are also simulated for comparison.

## 3-D Device Simulation Conditions

A 30nm NAND flash memory cell used in this work is shown in Fig. 3. $N_A$ has been varied from $1\times10^{17}$ to $3\times10^{18}$ cm$^{-3}$. Punch-through stopper (PTS) layer is adopted 30nm below the source/drain junction to suppress excess short channel effect. Monte Carlo simulations over 100 NAND flash cells are performed including RDF effect. Single trap at the channel interface is randomly placed. RTN amplitude $\Delta V_{th}$ is extracted from the constant current $V_{th}$ difference between trapped and de-trapped states (Fig. 1).

## Results and Discussions

$\Delta V_{th}$ against trap position along $L_g$ and $W$ for each $N_A$ is shown in Figs. 4(a)-4(j). At low $N_A$ up to $3\times10^{17}$cm$^{-3}$, it is found that $\Delta V_{th}$ is large at the center of the channel for both $L_g$ and $W$ direction. $\Delta V_{th}$ distribution peak for position along $L_g$ slightly locates near the source side since the drain voltage $V_D$ of 0.5V induces weak electrostatic potential asymmetry [1]. However, as $N_A$ increases, $\Delta V_{th}$ distribution peak along $W$ moves slightly towards the channel STI edges. Furthermore, extremely large $\Delta V_{th}$ is observed at the highest $N_A$ case. Figs. 5(a) and 5(b) show current density distribution of the channel surface near $V_{th}$ for the low and high $N_A$ device. For the low $N_A$ case (Fig. 5(a)), current widely flows at the center of the channel, corresponding to the $\Delta V_{th}$ spatial distribution in Figs. 4(b) and 4(d). On the other hand, in the high $N_A$ case (Fig. 5(b)), huge RTN is observed when the trap locates above the percolation current path formed by the random discrete dopants [1]. Figs. 6(a)-6(d) show $\Delta V_{th}$ spatial distribution in jellium doping case. The $\Delta V_{th}$ spatial distribution of the discrete doping case (Figs. 4(c) and 4(d)) is nearly the same as the jellium (Figs. 6(a) and 6(b)) indicating that very few dopants locate at the channel surface and hardly create percolation path when $N_A$ is low. As for the high $N_A$ case (Figs. 6(c) and 6(d)), $\Delta V_{th}$ is too optimistic where no outlier sample is observed. On the other hand, slight $\Delta V_{th}$ peaks near the STI edges are also observed in the jellium case (Fig. 6(d)), which is considered to be the electric field and current path concentration at the STI edge region [5].

Figs. 7(a) and 7(b) show $\Delta V_{th}$ probability distribution for jellium and discrete doping case, respectively. Distribution slope $\lambda$ cannot be determined below $N_A=2\times10^{18}$cm$^{-3}$ (Fig. 7(b)) as well as in the jellium case (Fig. 7(a)) since $\Delta V_{th}$ tail bits cannot be obtained due to the absence of percolation paths. Other physical origins should be considered such as multiple trap sites [6] or line edge roughness [7] to account for the $\Delta V_{th}$ tail bits found in the NAND flash memory measurement results [8]. Figs. 8(a) and 8(b) show $N_A$ dependence of the average and standard deviation of $\Delta V_{th}$, respectively. Average $\Delta V_{th}$ of the discrete doping case agrees well with the jellium, and continues to decrease as $N_A$ increases. However, standard deviation of $\Delta V_{th}$ starts to increase above $N_A=1\times10^{18}$cm$^{-3}$ in the discrete doping case since the channel becomes percolative around $V_{th}$.

## Conclusions

The spatial and statistical distribution of RTN in a 30nm node NAND flash memory in terms of $N_A$ are studied using 3-D Monte Carlo device simulation. Low $N_A$ in NAND flash memory results in large $\Delta V_{th}$ at the center of the channel region, showing jellium-like characteristics. Standard deviation of $\Delta V_{th}$ increases and $\lambda$ becomes available above $N_A=1\times10^{18}$~$2\times10^{18}$cm$^{-3}$, which is too high for NAND, when only considering RDF. Therefore, other physical origins should be considered to explain the $\Delta V_{th}$ tail bits in the previous NAND flash memory measurement reports.

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**References** [1] A. Ghetti et al., *IEEE Trans. Electron Devices*, vol. 56, p. 1746, 2009. [2] S. M. Amoroso et al., *IEEE Trans. Electron Devices*, vol. 59, p. 2774, 2012. [3] A. Ghetti et al., *IEEE Trans. Electron Devices*, vol. 59, p. 309, 2012. [4] A. Torsi et al., *IEEE Trans. Electron Devices*, vol. 58, p. 11, 2011. [5] W. Xiong et al., *SOI Conf.*, p. 111, 2003. [6] N. Tega et al., *IEDM*, p. 491, 2006. [7] L. Gerrer et al., *IRPS*, 3A.2.1, 2013. [8] D. Kng et al., *Symp. VLSI Tech.*, p. 206, 2011.

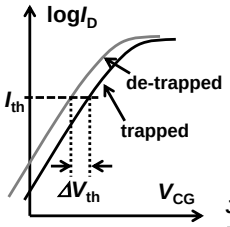


Fig. 1 Threshold voltage shift ($\Delta V_{th}$) by RTN.

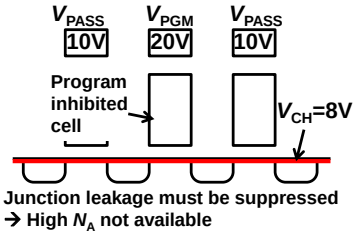


Fig. 2 Channel voltage ($V_{CH}$) boosting during program inhibit operation in NAND flash memory.

Table I Approach of this work.

| | NOR | NAND |
|---|---|---|
| $V_{PGM}$ | 10V | 20V |
| Max. channel voltage $V_{CH}$ during program operation | 5V (selected cell) | 8V (inhibited cell) |
| $N_A$ | high >1×10$^{18}$ cm$^{-3}$ | low ~3×10$^{17}$ cm$^{-3}$ |
| | [1] | This work |

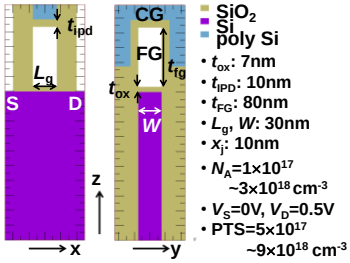


Fig. 3 Simulated 30nm NAND flash memory cell structure.

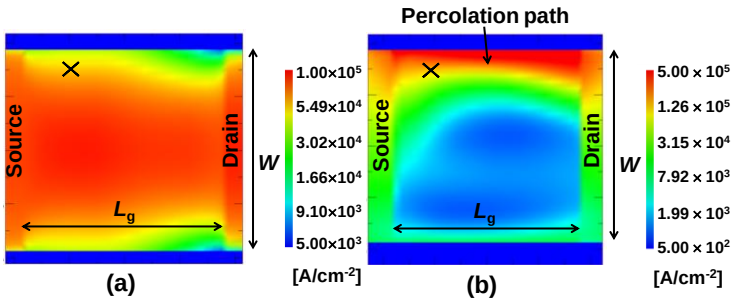


Fig. 5 Current density distribution at the channel surface of the de-trapped state near $V_{th}$. (a) $N_A$=1×10$^{17}$cm$^{-3}$. (b) $N_A$=3×10$^{18}$cm$^{-3}$.

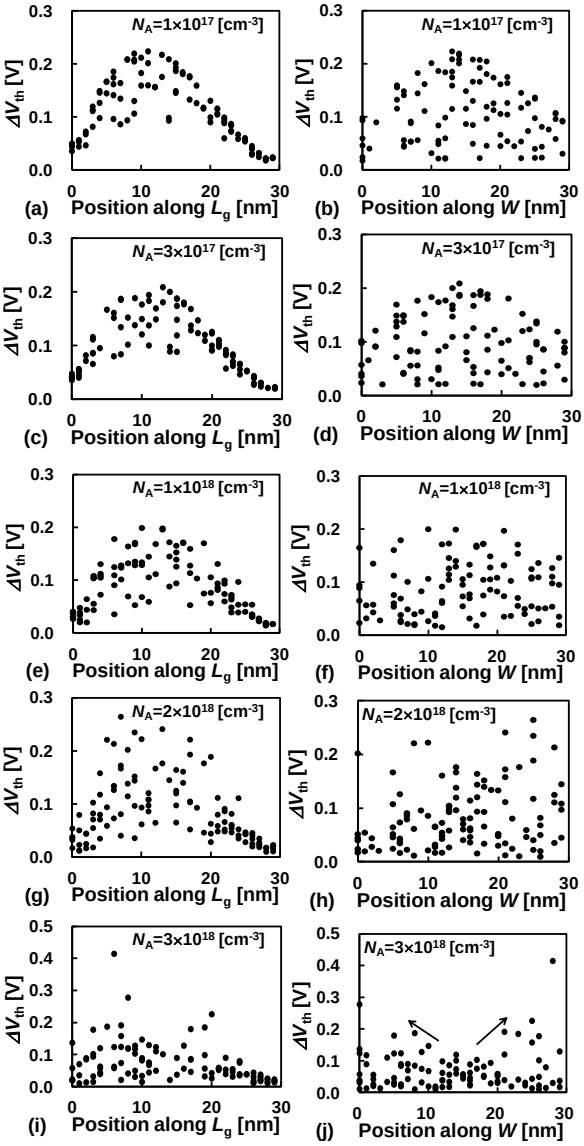


Fig. 4 $\Delta V_{th}$ against trap position along $L_g$ and $W$ for each $N_A$ in discrete doping case. (a), (b) $N_A$=1×10$^{17}$cm$^{-3}$. (c), (d) $N_A$= 3×10$^{17}$cm$^{-3}$. (e), (f) $N_A$=1×10$^{18}$cm$^{-3}$. (g), (h) $N_A$=2×10$^{18}$cm$^{-3}$. (i), (j) $N_A$=3×10$^{18}$cm$^{-3}$. For (a), (c), (e), (g) and (i), source edge is at 0nm.

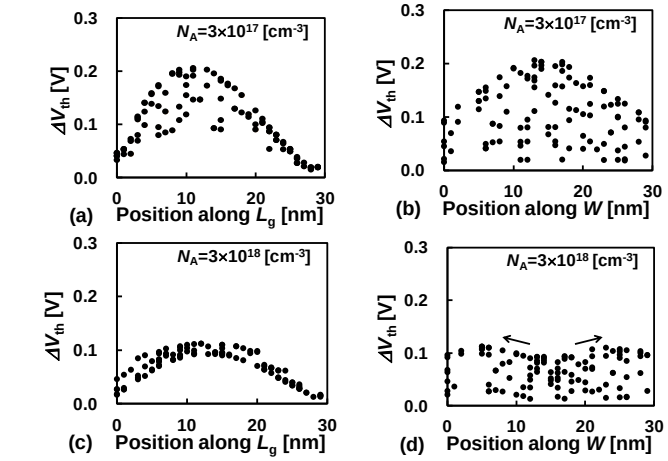


Fig. 6 $\Delta V_{th}$ against trap position along $L_g$ and $W$ for each $N_A$ in jellium doping case. (a), (b) $N_A$=1×10$^{17}$cm$^{-3}$. (c), (d) $N_A$= 3×10$^{18}$cm$^{-3}$.

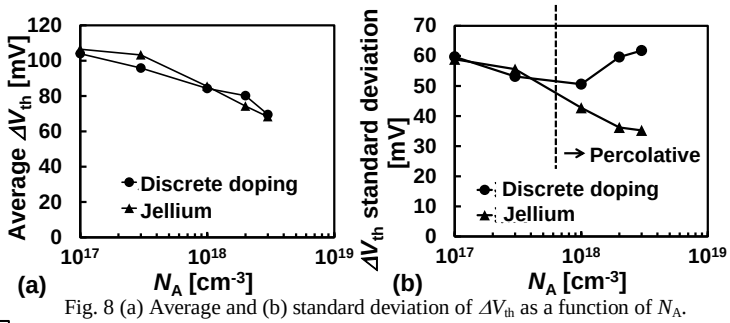


Fig. 8 (a) Average and (b) standard deviation of $\Delta V_{th}$ as a function of $N_A$.

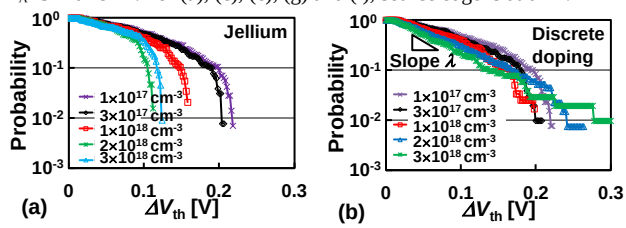


Fig. 7 Statistical distribution of $\Delta V_{th}$. (a) Jellium doping, (b) Discrete doping.