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Comparative Study of Floating Gate Type 3D Fin-Channel Flash Memories with Different Channel Shapes and Interpoly Dielectric Layers

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1. Introduction

The high-k interpoly dielectric (IPD) layer is essential for further scaling down of floating gate (FG) type flash memory to improve the gate coupling ratio [1, 2]. A high-k Al_2O_3 layer has been used as a blocking layer in charge trapping (CT) type planar and bulk FinFET flash memories [3-5]. However, the application of the high-k Al_2O_3 as an IPD layer for the FG type SOI-FinFET flash memory has not been investigated sufficiently. In this work, the high-k Al_2O_3 is introduced into the FG type 3D triangular-fin (TF) channel flash memories as shown in Fig. 1 for realizing a low-voltage operation due to the electric field enhancement at the sharp foot edges of a TF [6, 7]. Moreover, the dependences of fin shape and IPD layer material on the electrical characteristics of the fabricated FG type 3D fin-channel flash memories are comparatively investigated.

2. Device fabrication

To fabricate TF and rectangular-fin (RF) channels, we used (100) and (110) oriented SOI wafers. The ultrathin Si-fins were fabricated by using the orientation dependent wet etching [8], and the SiO_2 hard-mask on top of fins was removed by RIE to form triple-gate (TG) structure. After the fin formation, an 8-nm-thick tunnel oxide (T_{ox}) layer was formed by thermal oxidation, followed by the deposition of a 30-nm-thick n^+-ploy-Si layer as the FG material. After the FG formation, a 3-nm-thick SiO_2 layer was formed on the FG surface by rapid thermal oxidation (RTO), followed by a 5-nm-thick Si_3N_4 layer deposition by LPCVD. Then, an 8-nm-thick ALD-Al_2O_3 layer and a 7-nm-thick TEOS-SiO_2 layer were deposited on the different sample wafers for comparing. Finally, TiN control-gate (CG) formation, ion implantation (I/I), RTA and metallization were performed. To investigate the low-field gate leakage, large area multi-fin channel devices were also fabricated on each sample wafer.

3. Results and discussion

Figure 2 shows the SEM image of the fabricated FT device with an oxide-nitride-Al_2O_3 (ONA) IPD layer (TF-ONA) after CG formation. It is clearly confirmed that a 46-nm-gate is successfully fabricated. Figure 3 shows the cross-sectional STEM images of the fabricated TF-ONO, TF-ONA and RF-ONA devices. Note that almost the same size TFs and a 12-nm-thick RF are successfully fabricated thanks to the orientation dependent wet etching.

Figure 4 shows the measured I_d-V_g characteristics of the fabricated TF-ONA devices (50-cells) with the same L_g of 46 nm. Note that an excellent S-slope of 80-mV/decade is obtained thanks to the TG-structure. Figure 5 compares the statistical V_t variations of the fabricated 3 kinds of device. It is clear that TF-ONA device shows a smaller σV_t than the TF-ONO device due to the better uniformity of an Al_2O_3 layer than the TEOS-SiO_2. A slightly large σV_t in RF-ONA device should be resulted from the ultrathin fin width fluctuation. The I_d-V_g characteristics after one P/E cycle were also measured for all kinds of cell transistor, and the average memory window (MW) was also evaluated as shown in Fig. 6. The measured MW values are 4.3, 5.4 and 3.9 V for TF-ONO, TF-ONA and RF-ONA devices, respectively. The largest MW in TF-ONA device should be contributed by the high-k effect of Al_2O_3 and the improved charge injection efficiency due to the enhanced field at the sharp foot edges of a TF. Thanks to such effects, a low-voltage programing is achieved only in the TF-ONA device as shown in Fig. 7. Moreover, figure 8 demonstrates the channel hot electron (CHE) injection programing in TF-ONA device with L_g of 46 nm, which has been difficult to achieve in the planar-type NOR flash memories due to the low source-drain (SD) breakdown voltage beyond 100 nm L_g as shown in Fig. 9 [9].

Figure 10 compares the P/E characteristics of the fabricated 3 kinds of device at the same P/E condition. Note that a higher P/E speed, a larger memory window and a lower-voltage operation are achieved in the TF-ONA device as compared to the TF-ONO and RF-ONA devices. This result indicates that a high-k Al_2O_3 layer is very efficient for improving memory property due to the improved gate coupling, and the TF channel is very useful for the low-voltage operation as discussed before. The measured endurance characteristics of the fabricated 3 kinds of device are shown in Fig. 11. It is clear that TF-ONA device keeps a larger memory window as compared to the other devices up to 1 M-cycle operation. Figure 12 shows the measured data retention at room temperature and 85 °C. It is clear that data retention for all devices shows a weak dependence on the temperature. However, somewhat larger V_t shifts are observed in the RF-ONA and TF-ONA devices than TF-ONO ones. This indicates that such behavior should be related to the Al_2O_3-based IPD layer.

To clarify the origin of the large V_t shifts in RF-ONA and TF-ONA devices, we investigated the low-field gate leakage by using the fabricated multi-fin channel devices without FG layer, i.e., RF-MANOS, TF-MANOS and TF-MONOS, as shown in Fig. 13. Note that the larger gate leakage currents are observed in the RF-MANOS and TF-MANOS devices than TF-MONOS one, which should result in the somewhat larger V_t shifts in the RF-ONA and TF-ONA devices than TF-ONO ones. An abnormal gate leakage after 100 K-cycle operation is also observed in TF-MANOS device as shown in Fig. 14 (b). This behavior should be related to the deep traps in an Al_2O_3 layer [1]. To overcome such gate leakage, it is considered that adding a thin SiO_2 layer on top of an Al_2O_3 layer such as the bandgap engineered (BE) [10] IPD stack should be very efficient.

4. Conclusion

The scaled FG type 3D TF and RF channel flash memories with different IPD layers of ONA and ONO were successfully fabricated, and their electrical characteristics were systematically compared, for the first time. It was found that the TF-ONA device shows a higher P/E speed, a larger memory window and a lower-voltage operation as compared to the other devices thanks to the high-k of Al_2O_3 and the electric field enhancement at the sharp foot edges of a TF. Data retention in RF-ONA and TF-ONA devices should be dominated by the charge loss via the deep traps in an Al_2O_3 layer.

Acknowledgements

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References

[1] B. Govoreanu *et al., IEDM 2006*, p. 479. [2] H.-T. Lue *et al., IEDM 2011*, p. 203. [3] C. H. Lee *et al., IEDM 2003*, p. 613. [4] S.-K. Sung *et al., VLSI 2006*, p.106. [5] B. J. Tang *et al., IEDM 2011*, p. 219. [6] Y. X. Liu *et al., Jpn. J. Appl. Phys*, **51**, p. 06FF01. [7] R. Mih, et al., *VLSI 2000*, p.120. [8] Y. X. Liu *et al., VLSI2010*, p.101. [9] T-Y. Kim et al., *SNW 2005*. p. 98. [10] H.-T. Lue *et al., IEDM 2005*, p. 547.

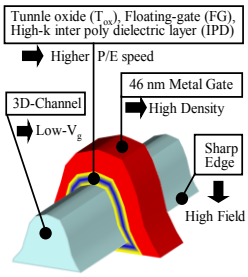

Fig. 1. Device structure of 3D fin-channel floating-gate (FG) type flash memory.

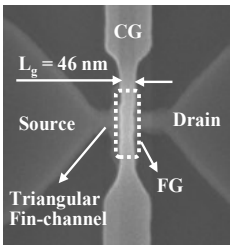

Fig. 2. SEM image of the fabricated floating-gate (FG) type triangular fin-channel flash memory with an ONA-IPD layer (TF-ONA).

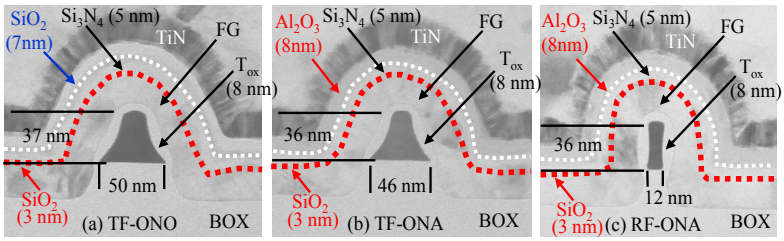

Fig. 3. Cross-sectional STEM images of the fabricated floating-gate (FG) type 3D fin-channel flash memories with different IPD layers and different fin shapes. (a) Triangular-Fin with Oxide-Nitride-Oxide (ONO) IPD layer (TF-ONO), (b) Triangular-Fin with Oxide-Nitride-Al_2O_3 (ONA) IPD layer (TF-ONA), and (c) Rectangular-Fin with Oxide-Nitride-Al_2O_3 (ONA) IPD layer (RF-ONA). A 30-nm-thick n^+ poly-Si layer was used as the FG material.

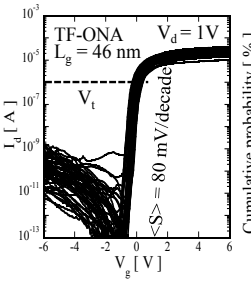

Fig. 4. Initial I_d-V_g of the fabricated TF-ONA devices with the same L_g = 46 nm.

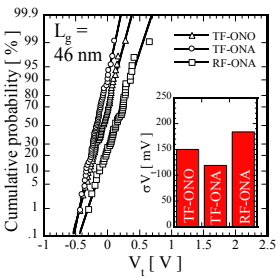

Fig. 5. Statistical V_t variations of the fabricated 3 kinds of device. Inset is comparison of σV_t values.

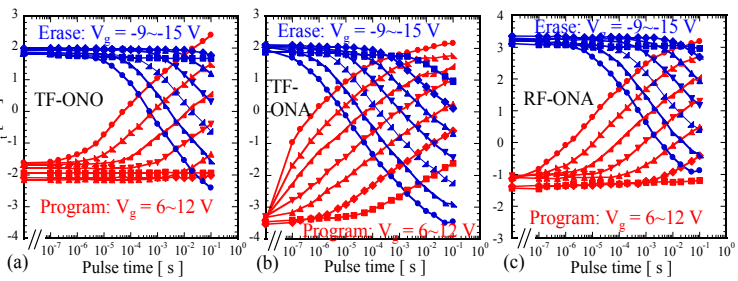

Fig. 10. P/E characteristics of the fabricated (a) TF-ONO , (b) TF-ONA, and (c) RF-ONA devices with the same L_g = 46 nm. It is obvious that TF-ONA device shows a higher P/E speed, a larger memory window and a lower voltage operation due to the high-k and sharp foot edges of a fin.

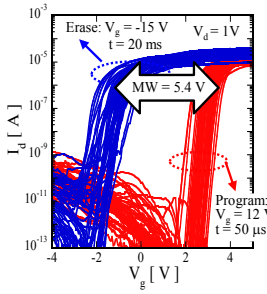

Fig. 6. I_d-V_g of the fabricated TF-ONA devices with L_g = 46 nm after one P/E cycle.

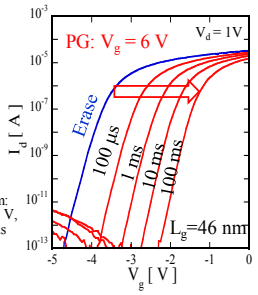

Fig. 7. Id-Vg of the TF-ONA device at V_g = 6 V programing with different pulse times.

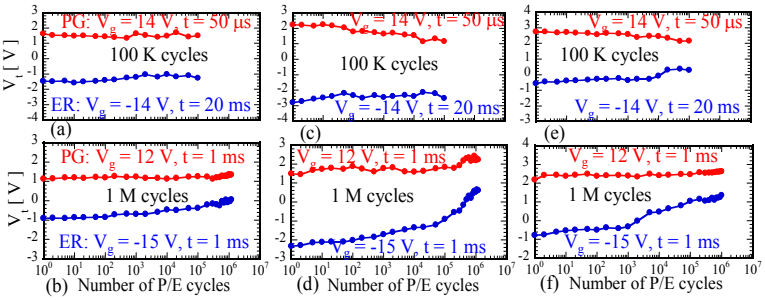

Fig. 11. Endurance characteristics of the fabricated (a)-(b) TF-ONO, (c)-(d) TF-ONA and (e)-(f) RF-ONA devices with the same L_g = 46 nm at different P/E conditions. The TF-ONA device keeps a larger memory window as compared to other devices up to 1 M-cycle operations.

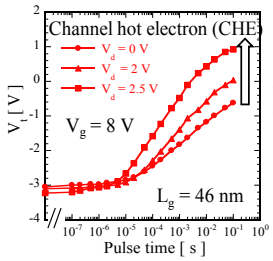

Fig. 8. CHE Programing of the TF-ONA device at different V_d values from 0 to 2.5 V.

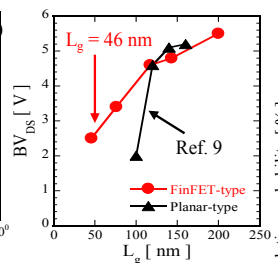

Fig. 9. Comparison of BV_{DS} between FinFET-type and planar-type flash memories.

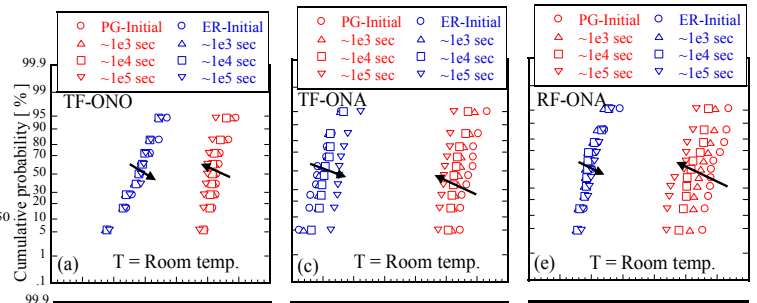

Fig. 12. Data retention of the fabricated (a)-(b) TF-ONO, (c)-(d) TF-ONA, and (e)-(f) RF-ONA devices with the same L_g = 46 nm at room temperature and 85 °C. Data retention for all devices shows a weak dependence on temperature.

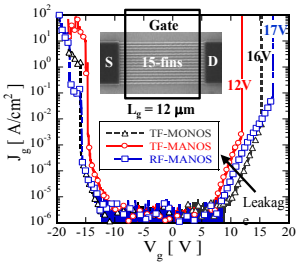

Fig. 13. J_g-V_g of the fabricated charge trapping type multi-fin devices. Inset is the SEM of the device after fin-EB.

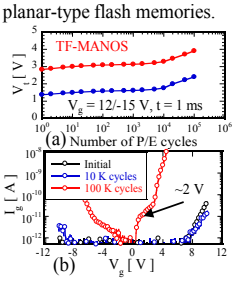

Fig. 14. (a) Endurance and (b) I_g-V_g of TF-MANOS before and after P/E cycles.