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A 0.94-THz Detector in 180-nm Standard CMOS Process

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Abstract

This paper proposes a CMOS terahertz detector implemented in 180-nm standard CMOS process. The detector consists of an NMOS filed effect transistor as rectifying element, an integrated on-chip patch antenna and a novel matching network. At 377-Hz modulation frequency, the measured voltage responsivity (R_v) and noise equivalent power (NEP) of the detector are 31V/W and 1.1nW/Hz$^{1/2}$, respectively.

1. Introduction

The terahertz (THz) frequency range of electromagnetic spectrum has a vast amount of potential applications in imaging. In early 1990s, Dyakonov and Shur theoretically demonstrated the possibility of using sub-micron field effect transistor as detector of terahertz radiation [1]. Emerging CMOS terahertz detector has attracted a great deal of attention because of their potential for low cost, high yield and easy integration. CMOS terahertz detector with an integrated silicon lens for 0.6 to 1 THz imaging was reported by Hadi and Sherry et al. in 2011 [2]. In 2012, a 1 k-pixel camera chip for active terahertz video recording has been fully integrated in a 65-nm CMOS bulk process technology [3].

This paper proposes a CMOS terahertz detector with a novel short stub matching network inserted between antenna and NMOS transistor. This detector achieves a voltage responsivity of 31V/W and an NEP of 1.1nW/Hz$^{1/2}$ with a 377-Hz chopper frequency at room temperature. It is shown that the detector can work well far beyond the used CMOS process cut-off frequency.

2. Detector

Fig. 1 (a) shows a schematic diagram of the proposed source driven detector based on an NMOS transistor with non-biased channel. The detector consists of an NMOS field effect transistor M1 (L=0.35μm and W=1μm) as rectifying element, an integrated on-chip patch antenna (76μm x 110μm) and a short-stub matching network MN. The input signal that received by antenna is directly transmitted to the source terminal of NMOS transistor Ml. Compared to the gate-driven mode [4], this source-driven configuration doesn't need additional tuning elements at drain terminal [2]. The rectified output signal is extracted from the drain node of the NMOS transistor. On-chip antenna and matching network are implemented in the top metal layer and the bottom layer is utilized to form ground plane. The insulator between patch and ground plane is 3.58μm thick. The structures of patch antenna and matching network are shown in Fig. 1 (b).

When THz radiation is coupled to the gate and source terminals of FET, the drain dc depends on the detected THz radiation power proportionally. The dc voltage ΔU can be written as [5],

$$\Delta U = \frac{U_a^{\,2}}{4U_0} \qquad (1)$$

where U_a is the amplitude of the ac voltage between gate and source induced by the incoming electromagnetic radiation and U_0 is the gate to channel voltage swing that is defined as $U_0=U_G-U_{th}$, where U_G is the gate voltage and U_{th} is the threshold voltage.

3. Proposed Matching network

To improve power transfer efficiency, we propose a short-stub matching network consisting of two transmission lines L1 (32.5μm x 1.98μm) and L2 (7.42μm x 1.98μm). The distance between transmission line L2 and antenna is 5.22μm. The end of transmission line L2 is connected to the ground plane. So this matching network not only matches impedance between antenna and NMOS transistor but also provides a dc path between the source terminal of the NMOS transistor and the ground. Compared to [2], this detector doesn't need extra source bias through the antenna, thus mitigating system-level complexity for future array implementing. A TCAD simulator is used to extract the input impedance of the NMOS transistor which is important for matching network design. The electrical performances of the antenna and the matching network have been simulated in the 3-D electromagnetic solver package HFSS.

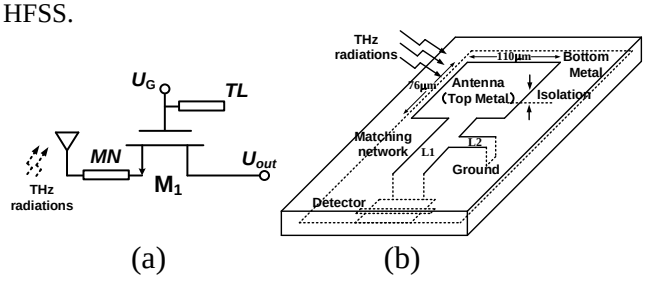

Fig. 1 (a) Schematic diagram of source driven broad-band detector and (b) structure of patch antenna and matching network

Considering the influence of the parasitic capacitance and inductance of bondwire on the input impedance of the detector, we add an open quarter-wavelength microstrip transmission line TL to the gate terminal of the NMOS

transistor (shown in Fig. 1 (a)). This transmission line provides a virtual ground point for RF while it forms an open for DC so that it has no impact on dc bias of the gate. To the best of our knowledge, this is first to consider the influence of bondwire with the current state-of-the-art in CMOS technology. The transmission line is also implemented using the top metal layer and the bottom layer is utilized to form ground plane.

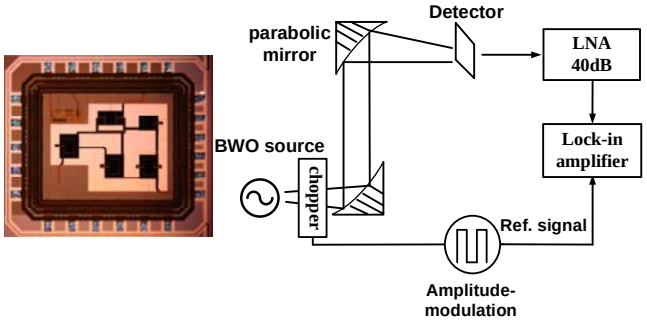

Fig. 2 (a) Chip die photograph and (b) measurement setup

4. Measurement Results

Fig. 2 shows the die photo of the 0.94-THz CMOS detector for testing (a) and the measurement setup for responsivity (b). A mechanical chopper with a frequency of 377Hz modulates a 942-GHz BWO source and at the same time generates TTL signal as the reference signal of a lock-in amplifier. The output signal is collimated and refocused into the detector by two parabolic mirrors. The output signal of the detector is amplified by a 40dB low noise amplifier (LNA). A lock-in amplifier, synchronized to the 377Hz source amplitude modulation signal, is used to capture the output of the LNA.

Fig. 3 shows the measured output voltage of the detector with 40dB gain of the LNA. The voltage responsivity R_v, defined as the ratio between the output voltage of detector and the power incident to the on-chip antenna, is calculated and plotted in Fig. 4. The peak responsivity is 31V/W at the gate bias voltage of 0.69V.

The noise equivalent power (NEP) is the ratio between the out noise voltage spectral density and detector voltage responsivity. In order to determine the NEP of the detector, output noise voltage spectral density is measured utilizing a LNA and a signal analyzer. The NEP versus gate bias voltage at 377-Hz modulation frequency is also shown in Fig. 4. The minimum NEP is 1.1nW/Hz$^{1/2}$ at 1.08-V U_g bias. At 0.69-V U_g bias, the NEP is 4.8nW/Hz$^{1/2}$.

5. Conclusions

This paper presents a 0.94-THz field effect transistor detector implemented in 180-nm standard CMOS. A novel short stub matching network inserted between antenna and NMOS transistor is proposed. This detector achieves a voltage responsivity of 31V/W and an NEP of 1.1nW/Hz$^{1/2}$ with a 377-Hz chopper frequency at room temperature. It is implied that this novel structure of the detector can be used in multi-pixel array for terahertz imaging.

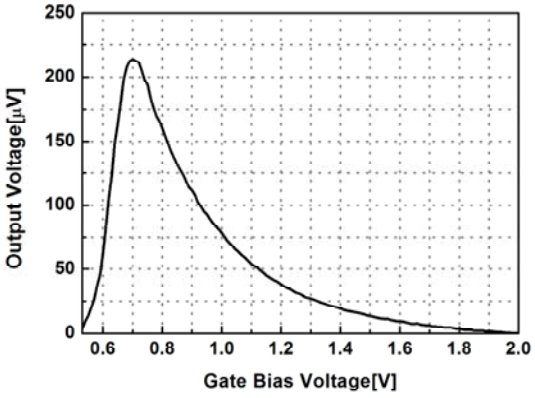

Fig. 3 Measured output voltage as a function of gate bias voltage

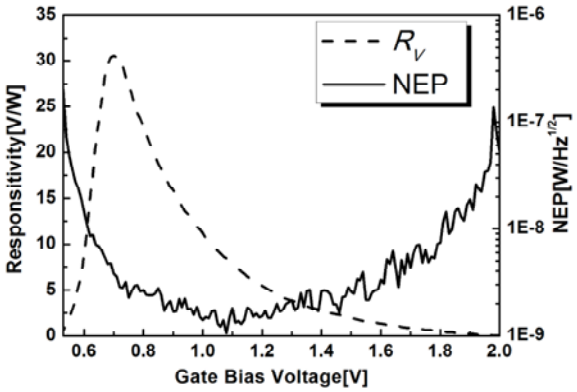

Fig. 4 Measured R_v and NEP for a sweep of gate bias voltage

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