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Luxtera's Silicon Photonics Platform for Transceiver Manufacturing

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Abstract

We present a commercial silicon photonics platform for the design and manufacture of high-performance optical transceivers, including a novel, wafer-scale light-source integration and packaging approach.

1. Introduction

By extending existing silicon design and manufacturing processes to include optical functionality, Si Photonics (SiP) leverages the enormous investment made in silicon integrated circuit design and manufacturing methodology over the past 40 years. In the past decade, several groups have reported excellent progress in SiP: ePIXfab/Ghent, Intel, IBM, IMEC and IME among others.

We report here on Luxtera's SiP platform, more than a decade in the making and now in its sixth year of commercial optical-transceiver /chipset production.

2. SiP Process & Device Library

Luxtera has developed two SiP processes: one at Freescale Semiconductor [1] and one at ST Microelectronics [2]. In both processes, we have developed a library of photonic devices that form the basic building blocks for our transceiver products. The libraries include all the functional elements needed to construct full-featured optical transceivers, including high-efficiency grating couplers optimized for coupling to and from single mode fiber.

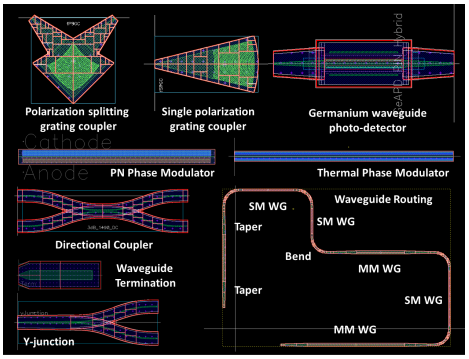

Fig 1 Various Si Photonic Library devices

A rigorous photonic device design verification methodology was devised to (1) establish behavioral models (including process, temperature and voltage corners) (2) ensure manufacturability of designs (3) establish reliability models (4) perform qualification tests per applicable standards [3].

3. Design Environment

We have developed a Cadence® based IC design environment [4] that includes: (a) an automated layout tool interfacing with the standard Cadence® layout tool allowing parameterized layout of photonic devices (b) a design rule check (DRC) tool enhanced with design rules for photonic device design, photonic device/process interactions and photonic/electronic interactions, (c) a layout-versus-schematic (LVS) tool extended with photonic capability ensuring optical and electro-optical connectivity (d) an end-to-end simulation tool based on Verilog-A behavioral models of the device library elements. Each device is described as a functional block with optical and electrical ports. Optical signals are described by their amplitude, wavelength and phase.

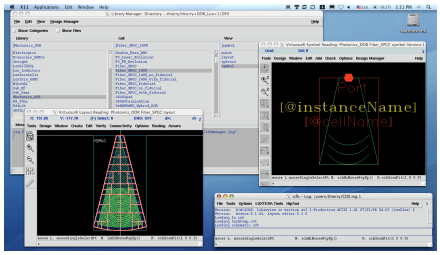

Fig 2 Physical layout and symbol of a library device.

The resulting PDK, with its automated DRC and LVS and full simulation capability is used in a manner completely analogous to pure electronic-PDKs and is an essential tool for the development of complex chipsets for optical transceivers.

4. Face-to-Face Chip Stacking

Previously, Luxtera's SiP transceivers were constructed using monolithically integrated electronics in the Freescale process. More recently, we have developed a hybrid integration approach using face-to-face die stacking with high-density, low-parasitic, copper-pillar interconnects. Both the Freescale and ST processes can be used in this scheme. This approach allows flexibility in the process node selection for the electronic circuits and enables integration with 3rd party IP and advanced CMOS nodes creating a roadmap gearing toward 50+ gigabaud. This flexibility is crucial, as advanced optical transceivers must incorporate many sophisticated electronic circuits to perform control, amplification, signal equalization, clock/data re-

covery, serialization/deserialization, etc.

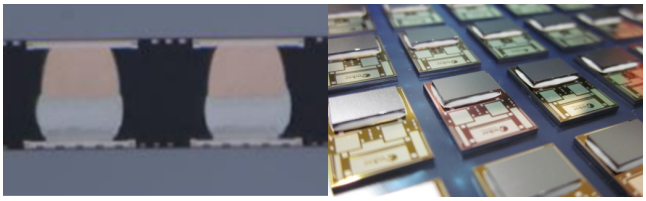

Fig 3 (left) low parasitic micro-bumps facilitate chip-to-chip stacking using, (right) Chip-to-chip assemblies of electronic dies on photonic dies prior to optical assembly.

5. Light Source

The laser light-source is a critical element for transceiver systems. Unfortunately, modern SiP processes currently offer no integral light source solution. Currently, all practical light sources for SiP involve some form of hybrid integration. In the literature several methods for light source integration have been reported [5][6][7]. Indeed Luxtera also explored many different options including: flip-chip lasers, TO-can packaged lasers and micro-packaged lasers. We describe here, as part of our platform, a now-mature hybrid, CW light-source solution employing a novel, micro-packaged commercial DBF laser-chip (see Fig 4 below). Since the modulation function is accomplished in the SiP chip, separate from the laser, it is possible to share a single CW laser across all the channels of a transceiver.

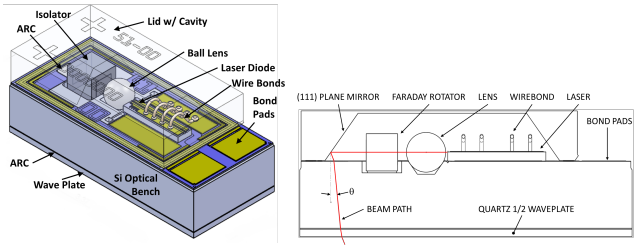

Fig 4 (left) Perspective view of hermetic silicon **La**ser **M**icro **P**ackage (LaMP), (right) section of LaMP showing beam path

In contrast to the other approaches mentioned above, the silicon micro-package design and wafer-level packaging platform enables the use of mature components (i.e. laser diodes, ball lenses and latching-garnet rotators) while simultaneously meeting stringent size, performance, cost and reliability requirements of SiP applications.

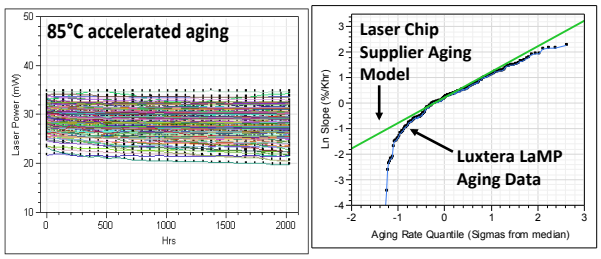

Fig 5 (left) Output power vs. time for LaMP devices aged as part of ongoing reliability studies, (right) Lognormal plot of LaMP aging rate replicating suppliers aging model

Using this packaging platform we have replicated laser-chip suppliers' aging and reliability in our LaMP device, see Fig 5.

6. Test Infrastructure

High-speed, automated *wafer-scale* test systems have been developed for both the LaMP and SiP wafers. The ability to perform, wafer-scale electro-optical testing enables high-volume manufacturing, and is essential for rapid development and optimization of photonic devices [1].

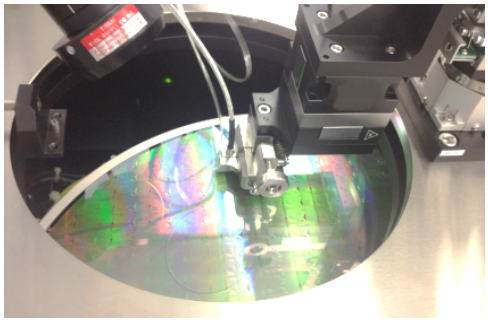

Fig 6 Wafer level optical test of 300 mm Si Photonics wafer using a commercial prober system enhanced with optical test capability.

Conclusions

We described a commercial Si Photonics platform suitable for the design and large-scale manufacture of advanced transceivers. This platform has been carefully constructed to allow rapid integration of more advanced silicon technology nodes and 3rd party IP. We presented a mature, pragmatic, wafer-scale, light-source packaging platform that allows the use of commercially available DFB lasers.

References

[1] A. Mekis et al., "A grating-coupler-enabled CMOS photonics platform," IEEE JSTQE, vol. 17, No. 3, pp. 597, May 2011

[2] Boeuf, F. et al." A multi-wavelength 3D-compatible silicon photonics platform on 300mm SOI wafers for 25Gb/s applications", IEEE International Electron Devices Meeting (IEDM) 2013 pp 13.3.1 - 13.3.4 2013

[3] S. Sahni et al., "Performance and reliability of a 25 Gb/s Ge waveguide photo-detector integrated in a CMOS process," in Proc. Electrochem. Soc., Las Vegas, 2010, p. 1931

[4] A. Mekis, et al. in "Silicon Photonics for Telecommunications and Biomedicine", S. Fathpour and B. Jalali, ed. [CRC Press, 2011]

[5] M. Heck, et. al, "Hybrid Silicon Photonic Integrated Circuit Technology", IEEE Journal of Selected Topics in Quantum Elec., 19, 4, July/August (2013)

[6] B. Koch, et. al, "Integrated Silicon Photonic Laser Sources for Telecom and Datacom", OFC/NFOEC Postdeadline Papers, PDP5C.8 (2013)

[7] E. Marchena, et. al, "Integrated Tunable CMOS Laser for Si Photonics", OFC/NFOEC Postdeadline Papers, PDP5C.7 (2013)