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# Process Control for Silicon Photonics using 300mm SOI wafers

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***Abstract*** *: We report results on the fabrication process control and device parameters control of a Silicon Photonics platform using a 300mm industrial fab.*

## 1. Introduction

In the last decade, the progress made by intensive academic and industrial research on basic Silicon Photonics buildings blocks paved the way for a large scale industrialization of performing and low cost optoelectronic transceivers. Recently several publications reported the development of industrial Silicon Photonics using 200mm process [1-3]. In this paper, we report some recent progress on the process control and device results of Silicon Photonics manufacturing using a 300mm CMOS production fab.

## 2. 25Gb/s Si Photonics Platform

Our Silicon photonics platform [4] is integrating electronics and photonics by using a 3D copper-pillars process (fig. 1). This allows a complete separation of the electronic IC (EIC) and the photonic IC (PIC) processes. As a consequence, different technologies can be used in order to optimize both processes. The PIC is fabricated using a 300mm production line.

## 3. 300mm Process Description and Control

Starting material is 300mm SOI wafer, featuring 310nm silicon thickness. Data taken from approximately 200 wafers are shown on fig. 3: wafer to wafer thickness range is about 4.25nm in the worst case that is approximately 5 X improvement versus existing 200mm wafer [5]. The within wafer uniformity full range is typical less than 2nm. The silicon layer in then patterned in two steps (fig.2). First, by using 193nm lithography, a partially etched silicon area is defined. This area is used for the definition of the optical passive components such as 1D and 2D surface grating couplers, monomode and multimode waveguides, directional couplers, bends etc. A second full-etch step is used to define optical isolation between components. The partial Silicon etch process control is key for optical device, especially for grating coupler control. Indeed, the spread of peak wavelength of grating couplers is directly proportional to the remaining Si-thickness variation, as shown on the wafer mapping of fig 4. By using 300mm tools we successfully reduced the remaining Si thickness range of 8nm that is an improvement of a factor of 2 versus existing 200mm processes. As a result our grating coupler design at 1310nm feature an average Peak Wavelength of 1309.64nm with a standard deviation of 2.42nm (fig. 5), measured on >350 samples. Further improvement on the remaining Si thickness control can be achieved by using a post process correction based on Gas Cluster Ion Beam (GCIB) [6], showing a intra wafer full range thickness control of 2nm (fig. 4) . Once Silicon patterning is finished, the lateral cladding is done using oxide filling and a CMP step. Next, P/N based optical phase modulators are fabricated using ion implantation. Typical overlay control for the P and N definition lithography takes advantage of 248nm lithography tools used in 300mm fab, with typical values measured on Silicon of +15nm/-15nm. High speed photodiode are fabricated using local silicon cavity etch followed by a selective Ge re-growth (fig. 6). Main source of process dispersion at this step are intra wafer: the standard deviation of the remaining Si thickness, measured within-wafer, after the cavity etch is less than 3%, and the Ge epitaxy thickness is controlled with a standard deviation of 5%. Finally, a 4 metal layers interconnects are deposited.

## 4. Device Performance and Control

Both 1310nm and 1490nm devices are supported, although the technology is compatible with 1550nm operation. Regarding the phase modulator, our process proposes two different flavors of modulator as show on fig 7 : two different tradeoffs between phase shift and insertion losses are available. The highest phase shift at 2.5V is 18°/mm that correspond to $V\pi L\pi$=2.5 V.cm, for an insertion loss of 6dB/cm. Regarding the high speed Germanium photodiode, a dark current less than100nA at -1V is obtained. An excellent wafer to wafer and intra wafer reproducibility is shown on fig.9, proving the robustness of the epitaxy process. The responsivity measured on 40 wafers is about 1A/W (fig. 8), with a wafer-to-wafer and within-wafer dispersion less that 10%. Finally the bandwidth statistics on several wafer is shown on fig. 10 showing a mean bandwidth about 20GHz at -1V, allowing a 25Gb/s operation.

## 5. Conclusion and Perspective

300mm wafer processing allows an excellent control of process variation especially suitable for Silicon Photonics, through improved starting material, lithography and etch control. Moreover, future generations of Silicon photonics will benefit of this process control capability, allowing the implementation of advanced device structures such as WDM, Photonic crystals etc.

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[2] S.Assefa et al., p. 33.8.1, pp 809-812, IEDM 2012
[3] D.J. Shin et al.,p. OTu2C.4, OFC 2013
[4] F.Boeuf et al., Proc. Of IEDM 2013
[5] S.K. Selvaraja et al., IEEE GFP 2011, pp 71-73
[6] N. Toyoda et al., GFP 2007, p58-60

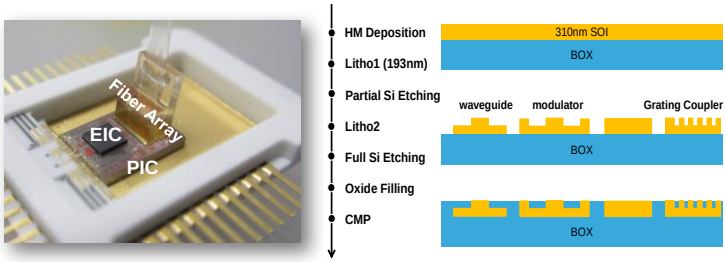


Fig.1 : 3D Silicon Photonics chip using Elec. IC over Photonic IC

Fig. 2 : process flow for optical passive components

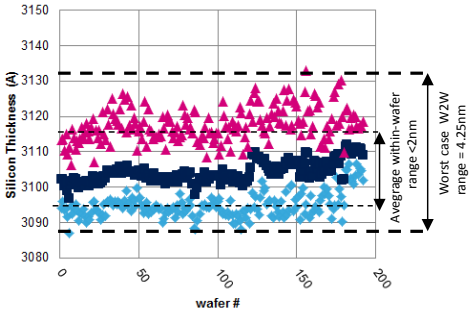


Fig 3 : Si thickness measurements showing min, media and max value per wafer (80 sites) for 200 wafers

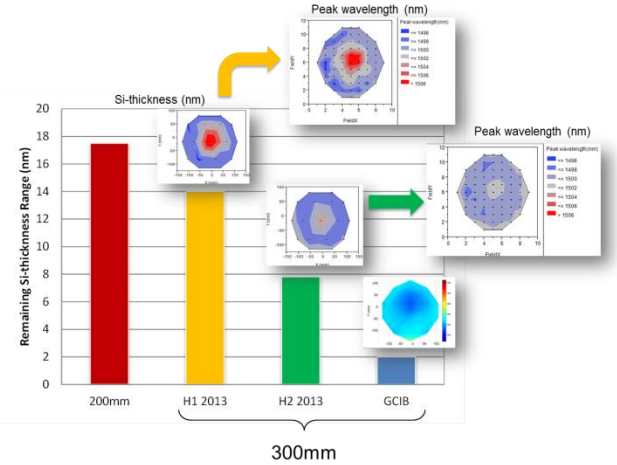


Fig. 4 : remaining Si thickness after partial ecth for 200mm, 300mm and post GCIB correction. Insert : correlation between Si thickness wafer mapping and peak wavelenth mapping of grating couplers

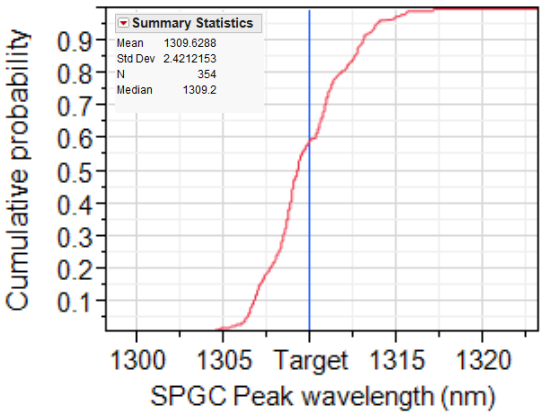


Fig. 5 : example of statistical distribution of the peak-wavelength of 354 grating couplers cumulated over different wafers and different lots.

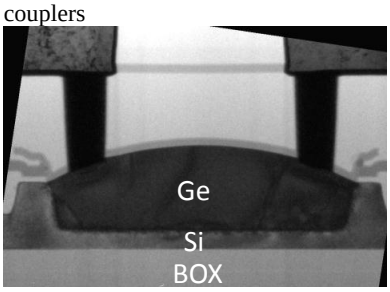


Fig. 6 : TEM cross section of Ge Photodiode

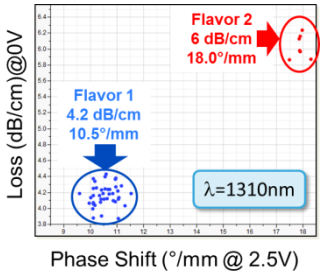


Fig. 7 : Loss/Phase shift tradeoff for High Speed Phase modulator flavors

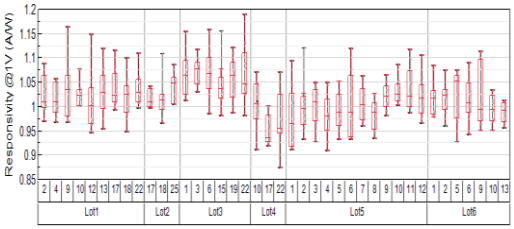


Fig.8 : Photodiode responsivity at 1310nm trend on 40 wafers from different lots

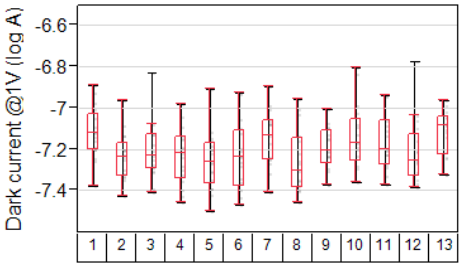


Fig. 9: Photodiode dark current trend on 13 wafers

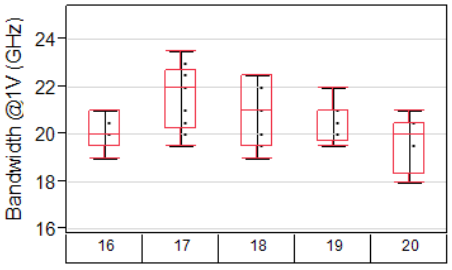


Fig. 10 : Photodiode bandwidth trend on several wafers