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Formation of Large-Grain Ge-Based Group-IV Crystals on Insulator by Seedless Rapid-Melting Growth in Solid-Liquid-Coexisting Temperature Region

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1. Introduction

To realize next generation system-in-displays, where high-performance LSIs are integrated with high-definition displays, high-speed thin-film transistors (TFTs) should be realized on insulating substrate, such as quartz. Since Ge-based group-IV materials such as Ge, SiGe, and GeSn have high carrier mobility, they are very promising as the channel materials of high speed TFTs. Thus, development of a technique for seedless formation of large-grain Ge-based crystals on insulator is essential.

We previously investigated the rapid-melting growth of pure *a*-Ge on insulating substrates such as quarts. However, grain-sizes of crystallized Ge films were limited less than ~5 μm. On the other hand, we achieved large-grain (≥100 μm) single-crystal Ge on insulator by combining artificial Si-seeding technique [1, 2]. These results show that if self-organized seed is formed on insulator, we can realize large-grain crystals without any artificial seeding technique.

Here, we focus on the phase diagrams of mixed materials of SiGe and GeSn. In these phase diagrams, solid-liquid-coexisting regions exist [Fig.1 (a)]. It is expected that, by annealing in these regions, materials partially melt, and thus, deviation into solid regions and molten regions occurs. Once cooling starts, the solid regions will work as seed for crystallization, and molten regions will lateral-epitaxially solidify from the seed.

In the present study, we examine this idea by investigating the annealing characteristics of a-SiGe-on-insulator and a-GeSn-on-insulator structures and realized very large grain growth of Ge-based group-IV crystals on insulating substrates.

2. Experiments

Si(100) wafers covered with Si_3N_4 films were employed. After a-$Si_{0.15}Ge_{0.85}$ or a-$Ge_{0.80}Sn_{0.20}$ films (thickness: 100 nm) were deposited, the films were patterned into strips (width: 3 μm, length: 100 μm) [Fig.1 (b)]. After deposition of SiO_2 capping layers (thickness: 800 nm), the samples were heat-treated by RTA (SiGe: 1070ºC, 1 sec; GeSn: 867ºC 1 sec). Here, these RTA temperatures exist in the solid-liquid-coexisting temperature regions [Fig.1 (a)].

3. Results and Discussions

Typical EBSD images of SiGe samples after RTA are shown in Fig. 2(a). As we expected, large grain crystal (~100 μm) was realized. However, the Si concentration profiles in the grown layers show laterally gradient [Fig. 2(b)]. This phenomenon can be explained by the growth model illustrated in Fig. 2(c). While heating at a temperature in solid-liquid coexisting region, phase deviation into Si-rich solid regions and Ge-rich liquid regions occurs (i). Once cooling starts, solidification of the Ge-rich liquid regions is initiated from the Si-rich solid regions, acting as seed, where solidification proceeds with generating Si segregation (ii). Consequently, lateral Si concentration profiles are formed in grown crystals, owing to the large segregation coefficient (k=3.1)[3] of Si in Ge (iii). The theoretically-calculated profiles of Si concentration [3] are shown by the dotted lines in Fig. 2(b), which agree well with the experimental results.

It is noted that the peak positions of Si concentration are different among these samples, as shown in Fig. 2(b). This is due to the different positions of self-organized seed in a-SiGe films. Such difference in the Si profiles should result in different electrical properties, which might be a problem from the application point of view.

To solve this problem, we came up with an idea to use Sn instead of Si. Here, the segregation coefficient of Sn in Ge is about 0.02 [4], which is much smaller than that of Si. Thanks to such a small segregation coefficient, we can expect that segregation during growth occurs strongly, and thus, almost all Sn atoms segregates to the edges of samples, and uniform-composition large crystals will be realized.

We investigate growth characteristics of a-GeSn samples to examine this idea. The EBSD image and concentration profiles are shown in Fig. 3(a). Large (~100 μm) grain crystals with uniform composition are obtained.

TEM images of the grown layer are shown in Fig. 3(b). This clearly indicates that the top- and bottom- interfaces of the layer are very flat, and no defects exist in the grown layer. These results evidence that large grain Ge-based crystals with uniform electrical properties are realized without any artificial seed by this technique.

4. Summary

Seedless rapid-melting growth of Ge-based group-IV mixed crystals has been investigated. By annealing at temperatures in the solid-liquid regions, group IV crystals with large lateral sizes are obtained. For SiGe case, grown layers show laterally concentration gradient due to the large segregation coefficient of Si. By selecting Sn instead of Si, almost all Sn atoms are segregated at edge of samples, and thus, uniform-composition large crystals are realized. This technique should be useful to realize high-speed TFTs for next-generation system-in-displays.

References

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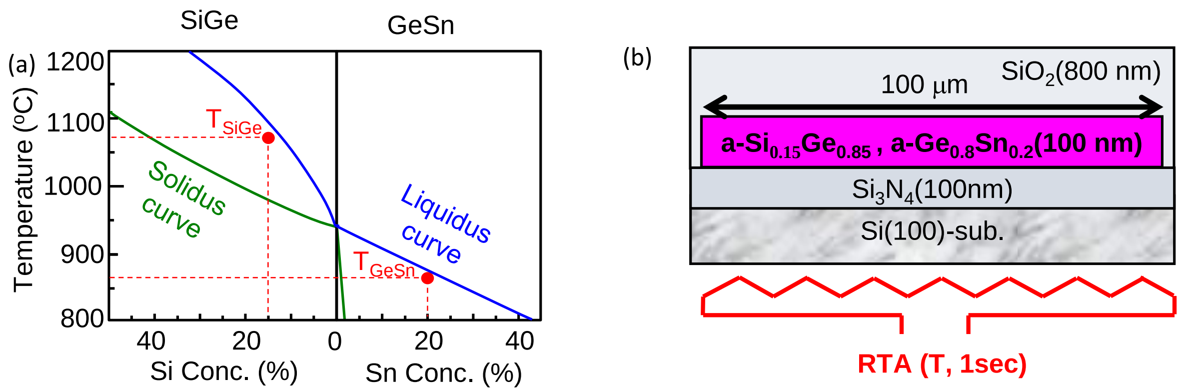

Figure 1 (a) Phase diagrams of SiGe and GeSn alloys. (b) Schematic sample structure. The RTA temperatures (T_{SiGe} and T_{GeSn}) are indicated in the diagrams.

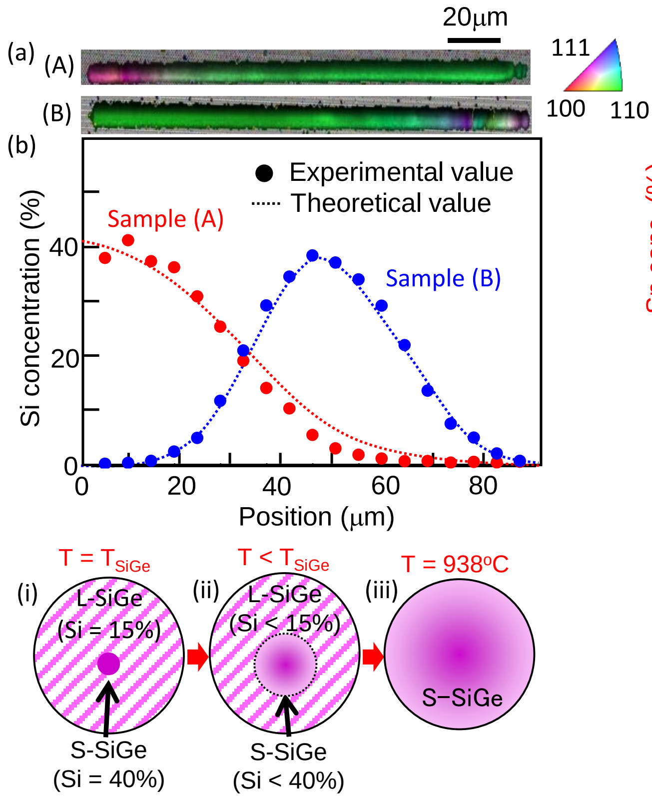

Figure 2 (a) EBSD images and (b) Si concentration profiles for SiGe samples after RTA. (c) Growth model of Si-gradient SiGe crystals. The Si concentration gradient is schematically shown by gradation of color.

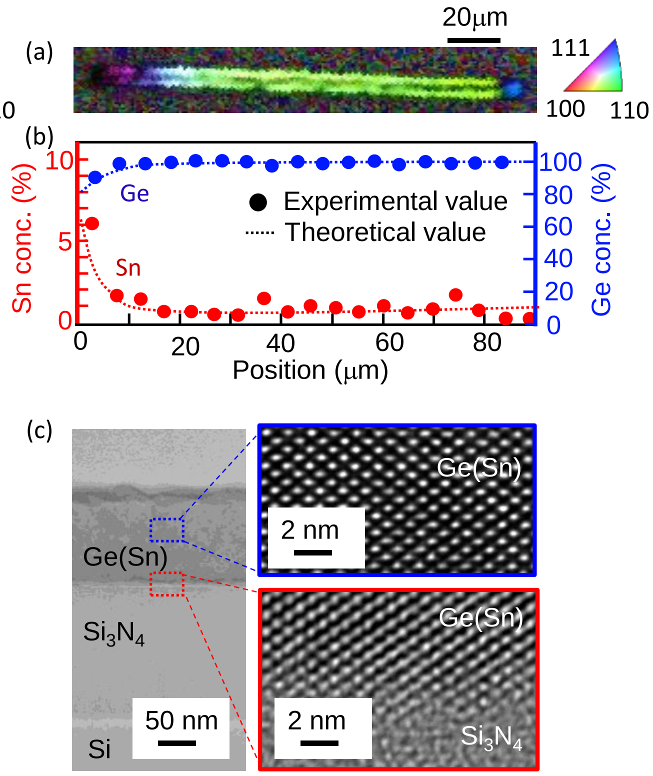

Figure 3 (a) EBSD image, (b) Sn and Ge concentration profiles, and (c) cross sectional TEM images for GeSn sample after RTA.