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Grain Growth Control by Micro-Thermal-Plasma-Jet Irradiation to Very Narrow Amorphous Silicon Strips and Its Application to Thin Film Transistors

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Abstract

Grain growth by micro-thermal-plasma-jet crystallization was controlled using very narrow amorphous silicon (a-Si) strips. With the decrease in strip width (W), grain boundaries were remarkably suppressed and no grain boundaries were formed at W= 0.3 μm. By applying high-pressure water vapor annealing (HWA) after crystallization, defect concentration was reduced to less than 5.0 x 10^{16} cm^{-3}, and as the result, significant improvements in mobility, threshold voltage (V_{th}) controllability, and off-current were achieved.

1. Introduction

In flat panel displays (FPDs), thin film transistor (TFT) is one of the most important devices. Hydrogenated amorphous silicon (a-Si) TFT has been widely utilized to the active-matrix backplane. However, for further increase in resolution and the integration of higher functionality, TFT with higher mobility and reliability are required. Therefore, new materials have been studied intensively now as candidates for next generation TFT channel. Low-temperature polycrystalline silicon (LTPS) TFT has attracted much attention because of their high field effect mobility (μ_{FE}), high reliability, and ability to integrate CMOS circuits. We have proposed the application of atmospheric pressure discharge micro-thermal-plasma-jet (μ-TPJ) to high speed lateral crystallization (HSLC) of a-Si films [1-3]. HSLC is induced by moving the molten region at very high speed of 4000 mm/s to form a lateral temperature gradient, which results in the long growth of ~100 μm [4]. In addition, we have attempted to control grain growth by μ-TPJ irradiation to a-Si pattern. Grain boundaries (GBs) were significantly suppressed with narrower strips [2]. TFTs fabricated by 2-μm-wide pattern achieved very high field-effect mobility (μ_{FE}) of 477 cm^2/Vs. In this work, we attempted to control the GBs by using a-Si strips with the width less than 1 μm, and electrical characteristics of crystallized Si strips were investigated. We also applied very narrow Si strips to TFT channels and investigated the electrical characteristics.

2. Experimental

Amorphous-Si films with the thickness (t_{Si}) of 100 ~ 250 nm were formed on a quartz substrate by plasma enhanced chemical vapor deposition using SiH_4 and H_2 at 250°C. Dehydrogenation was carried out at 450°C in N_2 ambient for 1 hour. A-Si films were patterned into strips of 0.1 ~ 4.5 μm in width (W) by electron beam lithography and chemical dry etching. To investigate defect state in Si strips, Si strips were lightly doped with channel doping concentrations (N_c = 5.0 x 10^{16} ~ 5.0 x 10^{18} cm^{-3}) by P^+ or B^+ before crystallization [5]. The μ-TPJ was generated by DC arc discharge under atmospheric pressure with a supply power (P) from 1.3 to 1.7 kW between a W cathode and a Cu anode with the spacing of 2.0 mm. The Ar gas flow rate (f) was varied from 1.0 to 3.0L/min. The μ-TPJ was formed by blowing out the thermal plasma through an orifice of 600 μm in diameter. The substrate was linearly moved by a motion stage in front of the μ-TPJ with a scanning speed of 2000 mm/s. The distance between the plasma source and the substrate (d) was varied from 1.8 to 2.3 mm. To measure current–voltage (I-V) characteristics of crystallized Si strips, Al electrodes were formed after formation of low resistance regions by implanting P^+ or B^+ (1.6 x 10^{20} cm^{-3}) and activation was carried out using μ-TPJ irradiation. Dopant types of strips and low resistance regions are the same in order not to form PN junction. N- and p-type top gate TFTs were also fabricated by following the process steps as reported in [4]. The maximum temperature throughout the TFT fabrication process was 450°C.

3. Results and discussion

Figure 1 shows the scanning electron microscope (SEM) images and crystallographic orientation map of crystallized Si strips after Secco-etching. GBs were remarkably suppressed with the decrease in W. Especially, Si strips with W= 0.3 μm were single crystals. Figure 2 shows the electrical conductivity (σ) of Si strips with respect to n-

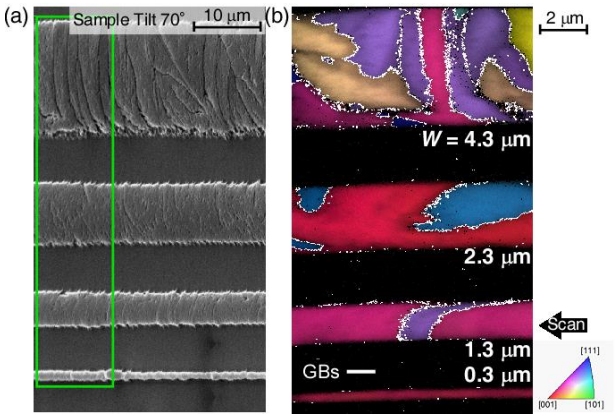

Fig. 1. (a) SEM image and (b) crystallographic orientation map of crystallized Si strips with different W.

(P^+) and p-type (B^+) doping concentration. Here, open circles show σ of as-crystallized strips and closed circles show that of same strips after defect reduction treatment by high-pressure water vapor annealing (HWA) [6]. In the case of p-type strips, they show relatively high σ, while n-type strips show significantly low σ when the doping concentration is below 5.0 x 10^{17} cm^{-3}. These results indicate that as-crystallized Si strips have intrinsic p-type nature due to donor-like states in lower half of band gap (Fig. 3). Although the crystallized narrow strips have no GBs and they are single-crystallized on the basis of electron backscatter diffraction (EBSD) observation, we have to interpret the behavior of σ that small amount of defects still exist. Since σ changes significantly when N_c is below 5.0 x 10^{17} cm^{-3}, it is suggested that n-type doping is compensated by the donor-like states due to electron trapping. After HWA, σ remarkably increased in all n-type strips because of effective termination of defects. This result indicates the defect concentration was reduced to less than 5.0 x 10^{16} cm^{-3} after HWA. It should be noted that even after the HWA, narrow strips with W = 0.3 μm showed highest σ value compared to wider strips. This indicates the defect concentration is the smallest in W = 0.3 μm strips. Furthermore, we investigated the effect of defect reduction on TFT characteristics. Figure 4 shows the transfer characteristics of n- and p-channel TFTs with channel doping. The channel doping of n- and p-channel TFTs were performed by B^+ and P^+ with N_c up to 1.0 × 10^{18} cm^{-3}, respectively. HWA was performed to all TFTs. As shown in figure 4 (a), large off-current was observed in the non-doped p-channel TFT, and it remarkably decreased with decreasing W and increasing N_c. In the case of W = 0.3 μm strip, V_{th} of p-channel TFT shifts to negative gate voltage by increasing the channel doping concentration. Similar tendency is observed in n-channel TFT. With the decrease in W from 4.5 to 0.3 μm, the μ_{FE} of n- and p-channel TFTs remarkably increased from 216 to 460 and from 90 to 193 cm^2/Vs, respectively. These results suggest that decreasing defects density in channel regions with narrower strips and HWA is quite effective to improve mobility and V_{th} controllability by channel doping. In addition, off-current of both channel TFTs with W= 0.3 μm were much lower than TFTs with W= 4.5 μm. From these results, combination of crystallization of very narrow strips and HWA is quite effective for CMOS operation with TFTs.

4. Conclusions

To control GBs in Si films crystallized by μ-TPJ, using very narrow a-Si strip and HWA is quite effective. Max μ_{FE} of 460 cm^2/Vs in n-channel and 193 cm^2/Vs in p-channel, V_{th} control by channel doping, and low off-current are achieved at W = 0.3 μm.

Acknowledgements

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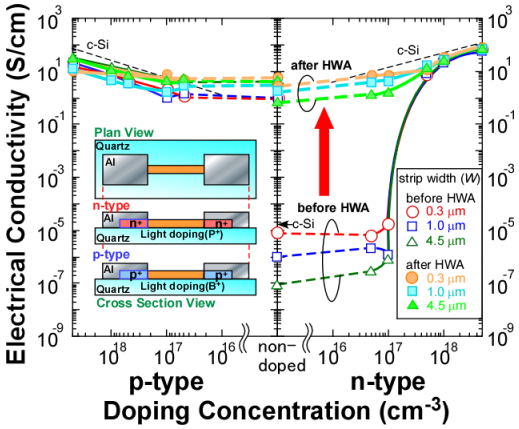

Fig. 2. Electrical conductivity of Si strips with different N_c.

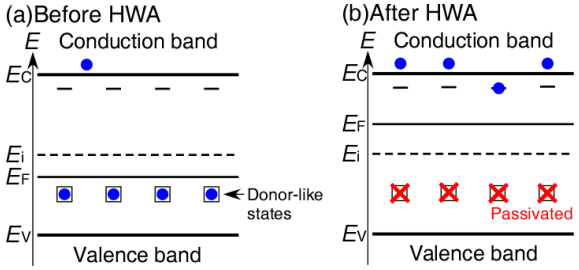

Fig. 3. Energy band diagram of crystallized Si strips (a) before and (b) after HWA.

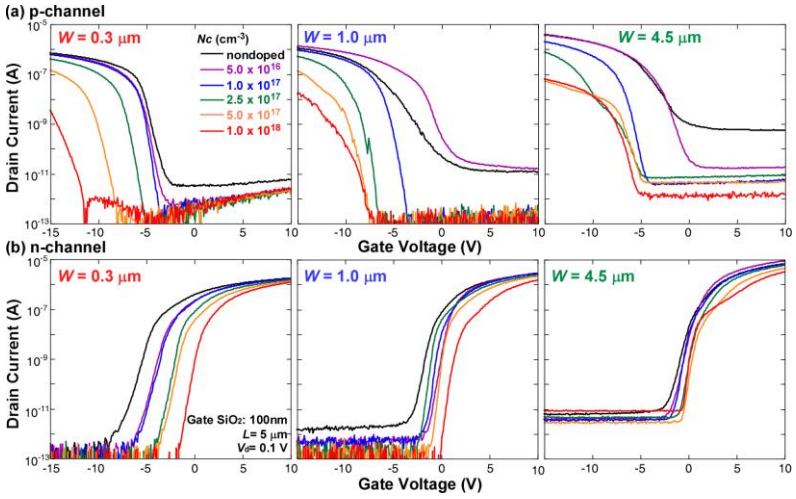

Fig. 4. Transfer characteristics of (a) p- and (b) n-channel TFTs with different N_c and W.