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Physical effects limiting performance and reliability of GaN High Electron Mobility Transistors

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Abstract

Recent results concerning Drain Current Transient Spectroscopy analysis of trap effects in GaN microwave and power devices are presented, identifying deep levels spatial and energy location. Reliability problems related with time dependent breakdown effects and threshold voltage instabilities are also presented.

1. Introduction

GaN-based High Electron Mobility Transistors (HEMT) present ideal characteristics for a variety of applications in wireless and satellite communication systems, radars, base stations and radio link transmitters. GaN heterostructure devices offer high channel current density with high mobility, and high breakdown voltage, thanks to the wide energy gap of GaN: consequently they enable power conversion with record efficiencies [1]-[3]. The full exploitation of the capabilities of this technology is currently hindered by trapping effects (causing current collapse in microwave HEMT and dynamic increase of on-resistance, Ron, in power devices), and by the still incomplete understanding of failure mechanisms that limit the safe operating area of GaN HEMT. This paper presents some recent results concerning the identification of deep levels and their effects in both microwave and power devices.

2. Pulsed measurements and Drain Current Transient Spectroscopy (DCTS)

The presence of trapping can be quickly analyzed by pulsed current-voltage characterization, starting from different quiescent bias points and driving both the gate and the drain voltages with suitable timing costraints. Dynamic changes of drain current I_D, transconductance g_m and threshold voltage V_T can be measured: deep levels within the epitaxial layers under the gate or at their interfaces exhibit predominantly V_T shifts, while the presence of traps in the gate-drain access region determines a dynamic decrease of the transconductance peak, with no significant modification of V_T. Pulsed I_D-V_D and I_D-V_G characterization, however, have a fixed time acquisition window (typ. 1 μs) and do not provide information on the dynamic behaviour and the nature of the trap states responsible for current collapse. In DCTS the drain is connected to V_{DD} through a load resistor; the device is kept in a defined trapping condition for 100s, and the subsequent transient investigation is carried out by switching the gate and by recording drain current response over at least eight time decades (e.g. from 1μs to 200 s) by means of an oscilloscope. Figure 1 depicts drain current transients recorded after trapping in different conditions.

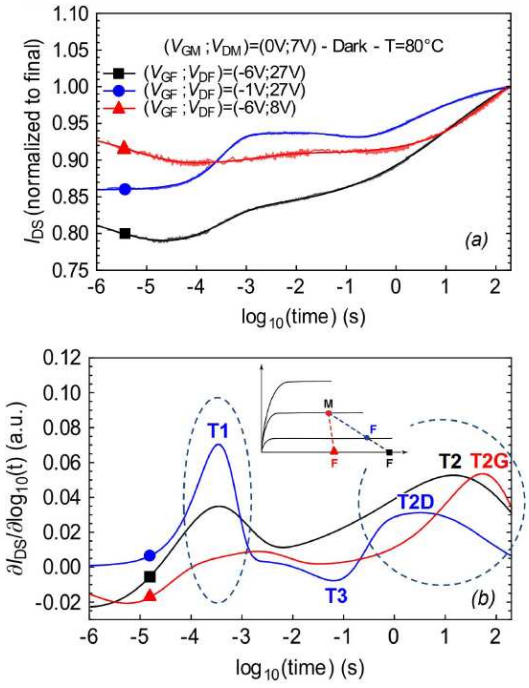

Fig. 1 Drain current transients recorded after trapping in different conditions (see insert).

Through the use of proper trap filling voltages it is possible to achieve information on the location of the traps. In general (but more complex situations may occur) traps located in the buffer can be charged either by hot electrons (trapping at high V_{DS} and/or relatively high I_D) or directly by the gate in the presence of conductive paths (due for instance to device degradation). Traps in the AlGaN can be both charged through gate leakage or by channel hot elec-

trons. Finally, trapping on the surface leads to dynamic degradation of extrinsic parameters without affecting V_T.

The "signature" of traps can be obtained by extrapolating the Arrhenius plot and evaluating activation energy E_a (eV) and cross-section σ (cm^2), taking into account device self-heating due to the dissipated power during measurements. A database containing data taken from more than 60 papers has been built, allowing one to directly compare measured data with literature and, on the basis of E_a and σ, make hypothesis on the physical origin of the traps [5]. In the following, we present several examples of the application of this methodology.

3. Role of buffer doping

AlGaN/GaN HEMTs were fabricated from three epitaxial wafers with identical structure but different levels of iron doping in the buffer, from undoped to $4x10^{17}$ cm^{-3}. Current collapse, due to a dynamic V_T shift towards positive values, was found to be correlated with Fe doping. DCTS revealed the existence of a trap level at 0.63 ±0.04 eV originated by an intrinsic defect clustering around dislocations, which was responsible for current collapse effects. The peak amplitude of this trap was directly correlated with the concentration of Fe in the buffer. Reverse bias stress of these devices induced an increase of gate leakage current, thus enhancing injection of electrons and charge trapping, leading to an increase of current collapse [6].

Appropriate buffer design is a key requirement for power switching GaN HEMTs, since it is critical for drain leakage current limitation, sharp pinch-off behaviour, and large off-state breakdown voltage. Compensation of unintentional n-type conductivity is usually accomplished using carbon. Small current-collapse and reduced R_{on} transients are present in optimized carbon doped devices, consistently with a C_N-C_{Ga} compensation mechanisms. On the contrary, 2D device simulations predicted large dispersion effects if C doping were dominated by acceptor states [7]. Recoverable threshold voltage instabilities have been observed in partially C-compensated devices [8]; simulations explain drain current transients (drain current high-pass behaviour followed by low-pass) as the result of two traps: an electron trap in the channel (0.11 eV from E_c) and a hole trap in the buffer, related to C doping (2.5 eV from E_c).

4. Trapping and reliability assessment of GaN power devices

Depletion-mode MISHEMTs were submitted to trapping experiments in off- or semi-on conditions [9]. In off-state experiments, trapping was found to induce an increase of the parasitic series resistance affecting R_{on} without V_T shift, due to a trap having Ea = 0.96 eV and $\sigma = 5.8 \times 10^{-15}$ cm^2. R_{on} increase was found to be proportional to the extension of the gate-drain region; consequently, trap location should be within the semiconductor access region and/or at the surface. Semi-on state testing induces a further deep level having Ea = 0.60 eV and $\sigma = 1.2 \times 10^{-17}$ cm^2; in the latter case, degradation is proportional to the drain current during the filling pulse, and is ascribed to hot electrons being trapped within the AlGaN or buffer layers adjacent to the 2DEG.

3. Reliability of GaN devices

Beside hot-electron degradation, microwave GaN HEMT have been shown to be prone to several failure mechanisms [6], including converse piezoelectric effects, time dependent gate breakdown, electrochemical GaN oxidation and pit formation. In power switching devices, high voltage bias may induce new failure mechanisms: (i) time-dependent drain-source breakdown, consisting in an uncontrolled increase of subthreshold I_D, without increase of I_G [11]; (ii) threshold voltage instabilities, due to the interaction between distinct traps in the undoped GaN channel and in the C-doped GaN buffer layer having different time constants [8].

3. Conclusions

Deep levels in GaN devices can be detrimental for both dynamic performance and device reliability. By controlling the evolution of trapping effects as a function of process conditions and material properties, significant improvements have been demonstrated for both microwave and power switching devices.

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References

[1] U.K. Mishra, L. Shen, T.E. Kazior and Y. -F. Wu, Proc. IEEE 96 (2) 287, 2008.

[2] N. Ikeda, Y. Niiyama, H. Kambayashi, Y. Sato, T. Nomura, S. Kato and S. Yoshida, Proc. IEEE 98 (7) 1151, 2010.

[3] D. Ueda, IEEE Int. Rel. Physics Symp. (IRPS), 3C.2.1, 2013.

[4] M. Meneghini, N. Ronchi, A. Stocco, G. Meneghesso, U. K. Mishra, Y. Pei, E. Zanoni, IEEE T. El. Dev 58(9) 2996, 2011.

[5] D. Bisi, M. Meneghini, C. de Santi, A. Chini, M. Dammann, P. Brückner, et al., IEEE T. El. Dev 60(10) 3166, 2013.

[6] M. Meneghini, I. Rossetto, D. Bisi, A. Stocco, A. Cester, G. Meneghesso, E. Zanoni IEEE IRPS 6C.6.1 2014

[7] G. Verzellesi, L. Morassi, G. Meneghesso, M. Meneghini, E. Zanoni, G. Pozzovivo, et al., IEEE EDL 35(4) 443, 2014.

[8] G. Meneghesso, R. Silvestri, M. Meneghini, A. Cester, E. Zanoni, G. Verzellesi, et al., IEEE IRPS 6C.2.1 2014

[9] M. Meneghini, D. Bisi, D. Marcon, S. Stoffels, M. van Hove, T.-L. Wu, S. Decoutere, G. Meneghesso and E. Zanoni, Appl. Phys. Lett. 104, 143505, 2014.

[10] M. Meneghini, G. Cibin, M. Bertin, G.A.M. Hurkx, P. Ivo, J. Sonsky, J.A. Croon, G. Meneghesso, E. Zanoni, IEEE Trans. El. Dev. 61(6) 1987, 2014.