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Record-Low Contact Resistance for InAlN/AlN/GaN HEMTs on Si with Non-Gold Metal

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1. Introduction

InAlN/GaN high-electron-mobility transistors (HEMTs) have great advantage over conventional AlGaN/GaN HEMTs due to the larger band gap discontinuity(ΔE_c~0.68eV)[1], which results in 2-3 times higher two dimensional electron gas (2DEG) density in the order of ~2.73x10^{13} cm^{-2}. Moreover, AlGaN/GaN HEMTs also face the strain induced reliability due to large (~18%) lattice mismatch between AlGaN barrier and GaN buffer layer [1]. Lattice-matched $In_xAl_{1-x}N$/GaN HEMT (x~0.17) mitigates strain-induced reliability due to the absence of piezoelectric polarization which helps to improve the overall device characteristics. By inserting a thin layer of AlN between InAlN barrier layer and GaN active buffer layer, the alloy disorder scattering is significantly reduced which in turn enhances the transport properties in the channel. The optimized heterostructure with gate length scaling and efficient process technique can provide improved DC and RF performances. Recently, Yue et al., achieved very high f_T/f_{max}=400/33 GHz with 30 nm-gate-length InAlN/GaN HEMT on SiC substrate with re-grown n$^+$-GaN and Au-based ohmic-contacts [2]. However, very few reports are available on InAlN/GaN HEMTs fabricated on Si substrate. Furthermore, most reported InAlN HEMTs devices were fabricated using conventional III–V gold-based ohmic metal schemes which is not compatible to existing Si process line [3]. Hence, non-gold ohmic contacts with low contact resistance (R_c) are essential for InAlN/GaN HEMTs to be manufacturable in the matured Si process line. Table I summarizes some of the best reported R_c values for ‘‘non-gold’’ based ohmic contacts for InAlN/GaN HEMTs on Si and SiC. Various non-gold ohmic metal stacks (Ti/Al/Ni [3], Ti/Al/Ni/W [4], Hf/Al/Ta [5], Ta/Al/Ta [6]) have been used by researchers to achieve low ohmic contact on InAlN/GaN HEMT. The lowest R_c of 0.56 Ω.mm so far achieved with annealing temperature at 900 °C for 60 sec [4]. Researchers at Chalmers Univ. also achieved R_c=0.64Ω.mm using Ta/Al/Ta metal stack on InAlN HEMT on SiC [6]. To further improve the R_c, we proposed a non-gold ohmic metal scheme using Ta with a thin-layer of Si layer for AlGaN/GaN HEMTs on Si substrate [7]. In this work, we have achieved a record-low R_c value of 0.36 Ω-mm in InAlN/AlN/GaN HEMTs on Si substrate using work function engineered ‘‘Ta/Si’’ based non-gold metal stack.

2. Experimental

The GaN HEMT structure was grown by metal–organic chemical vapour deposition (MOCVD) with a, 9-nm-thick $In_{0.17}Ga_{0.83}N$ barrier, 1-nm-thick AlN spacer layer, 1000-nm-thick *i*-GaN buffer and 100-nm-thick nucleation layer on high-resistivity Si (111) substrate [see Fig.1 (a)]. The grown structure exhibited room temperature 2-DEG mobility of 786 cm^2/V.s and sheet carrier density of 2.74×10^{13} cm^{-2}. After the formation of mesa isolation using dry etching by BCl_3/Cl_2 plasma, Ta/Si/Ti/Al/Ni/Ta (5/5/20/120/40/30 nm) ohmic metal was deposited and annealed at 825 °C for 30 s in a N_2 environment with a rapid thermal annealing (RTA) system.

Figure 1 shows the current-voltage characteristics of non-gold and gold-based ohmic contacts for InAlN/AlN/GaN HEMTs on Si substrate. Inset of Fig 1 shows the total resistance versus transfer length model (TLM) gaps. The conventional gold-based ohmic contact (Ti/Al/Ni/Au) on InAlN/AlN/GaN HEMT structure exhibited an average R_c as low as 0.33 Ω-mm and an average specific contact resistivity (ρ_c) of 3.27x10^{-6} Ω-cm^2. The non-gold ohmic contacts exhibited an average R_c as low as 0.36 Ω-mm with ρ_c of 4.47x10^{-6} Ω-cm^2 which is comparable with the gold-based ohmic contacts. The achieved R_c is believed to be the lowest ever reported for non-gold ohmic contacts on InAlN/AlN/GaN HEMTs on Si substrate and it is

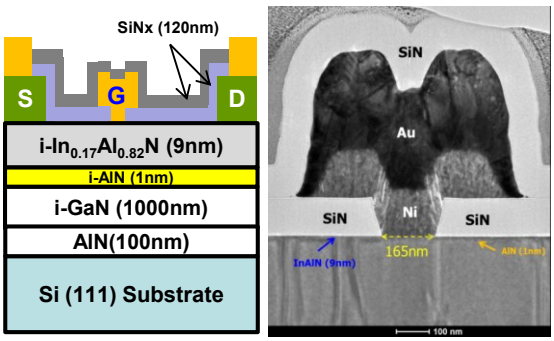

Figure 1.(a)Schematic cross-section (b) cross-sectional TEM image of T-gate on InAlN/AlN/GaN HEMT on Si substrate

Table I. Benchmarking InAlN/GaN HEMT on Si with non-gold ohmic contacts.

Affiliation	HEMT on Si	Ohmic Metal	Anneal Temp.(°C) /Time(sec)	Gate Metal	Rc [Ω.mm]
Alcatel [3]	InAlN/GaN	Ti/Al/Ni	800	Ta/Cu/Ta	1.53
IMRE [4]	InAlN/AlN/GaN	Ti/Al/Ni/W	900/60	RuOx	0.56
NUS [5]	InAlN/AlN/GaN	Hf/Al/Ta	600/60	-	0.59
Chalmers [6]	InAlN/AlN/GaN	Ta/Al/Ta	550/60	Ni/Au	0.64
This Work	InAlN/AlN/GaN	Ta/Si/Ti/Al/Ni/Ta	825/30	Ni/Au	0.36

also lower than that of InAlN/AlN/GaN HEMTs on SiC substrate [6]. Smooth surface morphology and good edge definition has also been observed which is similar to our non-gold ohmic contacts on AlGaN/GaN HEMT system [8]. A foot-print of 0.165-µm Schottky T-gate with 0.5-µm gate-head was formed with a metal stack of Ni/Au (150/400 nm) using electron beam lithography. Subsequently, the non-gold metal-stack Ti/Al/Ta (50/800/30 nm) was also formed as an interconnect metal. Finally, the devices were passivated with

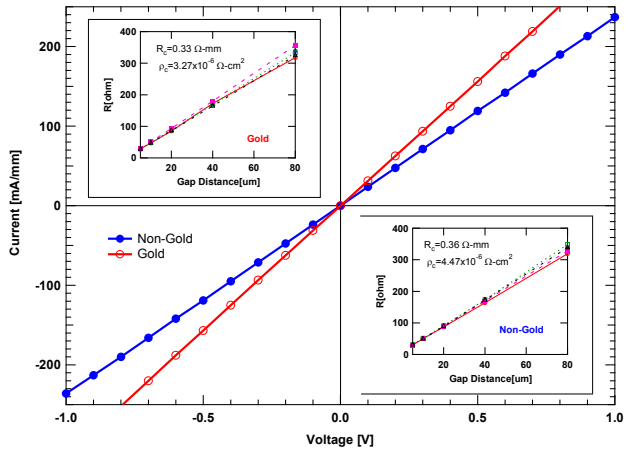

Figure 2. Current-Voltage characteristics of gold and non-gold ohmic contacts on InAlN/AlN/GaN HEMT with a gap of 5-µm (Width=50-µm). Inset: Total resistance versus TLM gaps for Gold (left) and Non-Gold (right) ohmic contacts

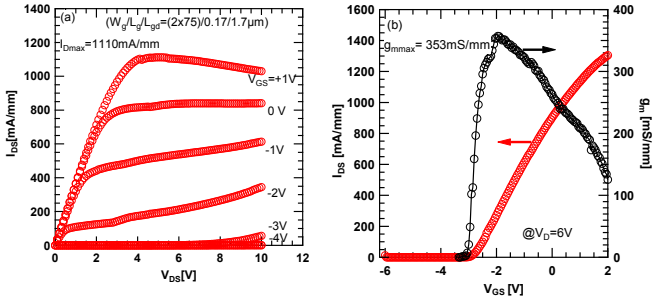

Figure 3. (a) I_{DS}-V_{DS} and (b) transfer characteristics of InAlN/GaN HEMTs ($W_g/L_g/L_{gd}$) = (2×75)/0.165/1.7 µm) on Si Substrate with non-gold ohmic contacts

120-nm-thick PECVD-grown SiN. The device dimensions used for this study are $L_{sg}/L_g/L_{gd}/W_g$=0.8/0.165/1.7/(2×75)µm. On-wafer DC and pulsed I–V characteristics of the HEMTs were measured using an Agilent B1500 semiconductor parameter analyzer and an Accent Diva D265, respectively. Microwave small-signal measurements were also carried out using an HP 8510c vector network analyzer (VNA).

3. Results and Discussions

Figure 2 shows the typical (a) I_{DS}–V_{DS} and (b) transfer characteristics of 0.165-µm gate length InAlN/GaN HEMTs. The fabricated HEMTs exhibited a maximum drain current density (I_{Dmax}) of 1110 mA/mm and a maximum extrinsic transconductance (g_{mmax}) of 353 mS/mm with a good channel pinch-off. The I_{Dmax} value is slightly smaller than the reported 1170 mA/mm for 50-nm gate length with source-drain spacing of 1.0-µm [6]. However, the reported device suffered from short channel effect and exhibited high output conductance beyond V_D=4V. Figure 3(a) shows the pulsed I_{DS}-V_{DS} characteristics (width=200ns, period= 1ms) of InAlN/GaN HEMTs on Si substrate with gate-lag (V_{gs0}=-5 V, V_{ds0}=0V) and drain-lag (V_{gs0}=-5V, V_{ds0}=10V) conditions. Very small (~8%) drain current (I_D) collapse was observed from the gate-lag (-5,0) and drain-lag (-5,10) at V_D=6V. The observation of small I_D collapse in gate-lag measurement is due to the lattice-matched InAlN/GaN HEMT structure, thus the absence of piezoelectric polarization. The strain-free InAlN barrier layer has also been verified by Leach et. al.[8]. In addition, the

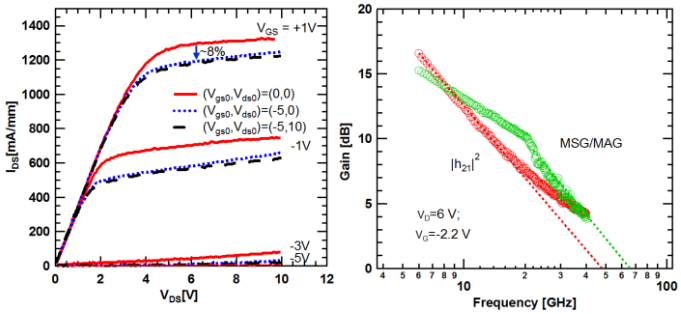

Figure 4. (a) Pulsed I_{DS}-V_{DS} characteristics (b) Small Signal characteristics of InAlN/AlN/GaN HEMT on Si substrate.

surface related current collapse is also suppressed by the optimized SiN passivation with ammonium sulphide pre-treatment [9,10]. Figure 3 (b) shows the two-terminal gate Schottky diode characteristics. The reverse gate leakage current of the device measured at V_G= -15V was 1.6×10^{-2} mA/mm which is typical for Ni/Au Schottky gate InAlN/GaN HEMTs. The device exhibited a Schottky barrier height of 0.81 eV with an ideality factor of 1.38. Figure 4(b) shows the small-signal microwave performance of InAlN/GaN HEMTs measured at V_g=-2.2V and V_D=6V. Table II shows the measured DC and small signal parameters for InAlN/GaN HEMTs using gold- and non-gold-based ohmic contacts.

Table II. Device DC parameters of InAlN/GaN HEMTs with gold and non-gold ohmic contacts: $W_g/L_g/L_{gd}$ = (2×75)/0.165/1.7 µm)

Ohmic metal	R_c (Ω.mm)	I_{Dmax}[mA/mm]	g_{mmax} [mS/mm]	f_T/f_{max}[GHz]
Ti/Al/Ni/Au	0.33	1320	363	64/72
Ta/Si/Ti/Al/Ni/Ta	0.36	1110	353	48/66

4. Conclusion

We have demonstrated for the first time 0.165-µm gate-length InAlN/GaN HEMTs on Si substrate with promising device performances using a non-gold metal stack. Ta/Si-based ohmic contact exhibited lowest R_c=0.36 Ω-mm with smooth surface morphology, This is comparable to the gold-based ohmic contact on the same device structure. The fabricated HEMTs exhibited I_{Dmax} of 1110mA/mm, g_{mmax} = 353mS/mm, I_D collapse of <8%, f_T=48 GHz and f_{max}= 66 GHz. These results demonstrate the feasibility of using non-gold metal stack as a low R_c ohmic contact to achieve good performance submicron-gate InAlN/AlN/GaN HEMTs on Si substrate for high-frequency applications.

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