Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp634-635

Impact of $In_{1-x}Ga_xAs$ Capping Layer on Characteristic of III-V Trigate MOSFET Devices

Cheng-Hao Huang[1,2] and Yiming Li[1,2,3,*]
[1] Parallel and Scientific Computing Laboratory, National Chiao Tung University, Hsinchu 300, Taiwan
[2] Institute of Communications Engineering, National Chiao Tung University, Hsinchu 300, Taiwan
[3] Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu 300, Taiwan
*Tel: +886-3-5712121 ext. 52974; Fax: +886-3-5726639; Email: ymli@faculty.nctu.edu.tw

Abstract

In this work, we study the impact of channel capping layer on III-V trigate MOSFET. 3D device simulation shows that the 14-nm device with $In_{1-x}Ga_xAs/In_{0.53}Ga_{0.47}As$ channel has large driving current owing to small band gap and low alloy scattering at the channel surface. The mole fraction (x) of Ga, varying from 0.27 to 0.42, and the thickness of capping layer $In_{1-x}Ga_xAs$, ranging from 3 to 5 nm, are studied for device DC characteristic. The device with a 4-nm-thick $In_{0.68}Ga_{0.32}As$ capping layer is promising for advanced device applications.

1. Introduction

High-speed device can be realized by using InGaAs related materials owing to their high electron mobility [1-2]. Recent studies on III-V FETs have shown fascinating characteristic from thin-channel planner MOSFETs [3-4]. III-V junctionless FET devices have also been reported for even superior on/off behavior and current ratio [5-6]. InGaAs/InAlAs is one of highly attractive III-V materials due to lattice match [7] and outstanding heterojunction transport property [8]. III-V transistors with high electron mobility will increase the drive current, but the leakage current will also increase. Consequently, proper channel capping layers [9-11] will benefit device applications. III-V devices with vertical channel and capping layer will be an interesting study.

In this work, we study the impact of the thickness (T_{cap}) and the mole fraction (x) of Ga of capping layer on DC characteristic of 14-nm $In_{1-x}Ga_xAs$ / $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ / InP trigate MOSFETs. Notably, owing to similarity in materials of capping layer $In_{1-x}Ga_xAs$ and channel layer $In_{0.53}Ga_{0.47}As$, the explored new device could be fabricated. By considering the short-channel effect (SCE) parameters: $I_{on}/I_{off} > 1.7\times10^6$, subthreshold swing (SS) < 72 mV/dec, and drain induced barrier lowering (DIBL) < 55 mV/V simultaneously, we find the feasible range of T_{cap} and x for high-performance device applications, where the threshold voltage (V_{th}) is targeted at 160 mV.

2. The Device Configuration and Simulation

Figure 1(a) illustrates a process flow for fabricating the explored III-V device. 3D process simulation is performed to simulate device structure and doping profiles. A list of fabrication steps is shown in Fig. 1(b). The sample is grown by metal oxide chemical vapor deposition on Si substrate; first, 1-μm-thick InP is deposited then 1.5-μm-thick p-type doped 1×10^{15} cm^{-3} $In_{0.52}Al_{0.48}As$ buffer layer is followed, and undoped $In_{0.53}Ga_{0.47}As$ channel layer is applied. The channel capping layer of $In_{1-x}Ga_xAs$ with different x and T_{cap} is covered with $TaSiO_x$. Source/drain is selectively doped by Si and activated by rapid thermal anneal (RTA). Ni is deposited as gate electrode by reactive sputtering. S/D metal is defined by e-beam evaporation and lift-off process. Figure 2(a) shows a 3D-plot of the InGaAs-based trigate MOSFET and Fig. 2(b) is a cross-sectional view along the cutting line AA', where the intrinsic channel is of $In_{0.53}Ga_{0.47}As$ with a capping layer of $In_{1-x}Ga_xAs$. The adopted parameters are listed in Fig. 2(c), where T_{cap} varies from 0 to 5 nm and x is from 0.27 to 0.42. To minimize the random dopant fluctuation, undoped $In_{1-x}Ga_xAs$ capping layer above channel is studied. Optimal capping layer of $In_{1-x}Ga_xAs$ will be discussed subject to the aforementioned SCE parameters. 3D quantum transport device simulation is performed for carrier transport. The mobility degradation due to high normal field and alloy scattering is considered. The acceptor-liked traps are placed at the high-κ gate oxide-InGaAs interface.

3. Results and Discussion

The energy bands, as shown in Fig. 3, is first plot for both the on- and off-state. The conduction band energies are reduced near surface when the thickness of $In_{1-x}Ga_xAs$ capping layer is increased, as shown in Fig. 3. Zoom-in plots of Figs. 3(a) and (b) clearly show that the conduction band energies of T_{cap} = 4 nm are lower than that for T_{cap} = 0 nm owing to the low energy band gap. All energies of the off-state are above Fermi level, so the III-V device is normally off. For the on-state, as shown in Fig. 3(b), the conduction band and Femi level of electrons become negative. The electron's Fermi levels are above conduction bands, so the regions between electron's Fermi level and conduction band are filled with electrons. The conduction band energy is low, so the device with T_{cap} = 4 nm has large electron concentration and the on-state current.

Figure 4 shows I_D-V_G and transconductance (g_m-V_G) curves with T_{cap} = 4 nm and different Ga concentrations. Devices with low Ga concentration show high driving current, resulting from an improved mobility. The lattice constant of InGaAs with Ga mole fraction of 0.47 is 0.586 nm, which matches with that of $In_{0.52}Al_{0.48}As$. For x < 0.47, the lattice constant of the capping layer is larger than 0.586 nm and the channel is subjected to a compressive strain. As the compressive strain increases, the alloy scattering decreases, resulting in improved electron mobility. As shown in Figs. 5(a) and (b), we plot the I_D-V_D characteristics. It is obviously to see that drive current of the device without capping layer is the lowest in Fig. 5(a). Fig. 5(b) shows that devices with a small x will have large driving current. They are because the large region of small band gap and high mobility will decrease the S/D resistance. On the other hand, devices with thick capping layer and low Ga concentration have the large gate capacitance (C_G), as shown in Figs. 5(c)-(d). Large C_G induces large inversion charge thereby enhancing the current density. Therefore, devices with thick T_{cap} of $In_{1-x}Ga_xAs$ and low x may possess the better gate controllability.

Figure 6 shows the electron density profiles at the on-state for different x and T_{cap}. No matter increasing the thickness of capping layer or decreasing the gallium concentration, the centroid of the inversion charge density in the channel is pulled toward the gate oxide interface; consequently, they will induce high electron density and increase the on-state current. This phenomenon increases the gate control over the channel thereby reducing the impacts of short channel effect. Thus, to get the optimal design of capping layer, we plot the figures about SS, DIBL, I_{on}/I_{off} and V_{th} versus the x and T_{cap} to observe the trends, as shown in Fig. 7. Both SS and DIBL decrease with T_{cap} increase and x decrease are plotted in Figs. 7(a)-(b). However, although the on-state current increases due to small band gap and high mobility, the off-state current also increases thereby a trade-off existing for the on/off current ratio, as shown in fig. 7(c). Finally, if a V_{th} of 160 mV is considered for high-performance application, a 4-nm thickness of $In_{1-x}Ga_xAs$ capping layer with x = 0.32 could be optimized accordingly.

3. Conclusions

In summary, we have studied the impact of T_{cap} and x of $In_{1-x}Ga_xAs$ capping layer on 14-nm $In_{1-x}Ga_xAs$ / $In_{0.53}Ga_{0.47}As$ / $In_{0.52}Al_{0.48}As$ / InP trigate MOSFET. For the given specifications of SS < 72 mV/dec, the on-/off-state current ratio > 1.7×10^6, DIBL < 55 mV/V with V_{th} = 160 mV, the device with a 4-nm $In_{0.68}Ga_{0.32}As$ capping layer may provide optimal characteristic for high-performance device applications.

Acknowledgement

This work was supported in part by Taiwan National Science Council (NSC) under Contract NSC-102-2221-E-009-161.

References

[1] J. A. del Alamo et al., in: *IEDM Tech. Dig.*, 2013, p. 21.
[2] C.-S. Shin et al., *VLSI Symp. Tech. Dig.*, 2014, p. 36.
[3] J. A. del Alamo, *Nature*, 479, 2011, p. 317.
[4] S.-H. Chen et al., *Nanoscale Research Letters*, 7, 2012, p. 431.
[5] J. P. Colinge et al., *ECS Transactions*, 35, 2011, p. 63.
[6] J. H. Seo et al., *Semicond. Sci. Technol.*, 28, 2013, p. 105007.
[7] I.-H. Ahn et al., *Jpn. J. Appl. Phys.*,49, 2010, p. 084303.
[8] A. V. Thathachary et al., in: *Proc. DRC*, 2013, p. 17.
[9] Y. Takano et al., *Jpn. J. Appl. Phys.*, 49, 2010, p. 105502.
[10] H.-C. Chin et al., *IEEE Electron Device Lett.*, 32, 2011, p. 146.
[11] Y. Li et al., *J. Comput. Electron.*, 5, 2006, p. 255.

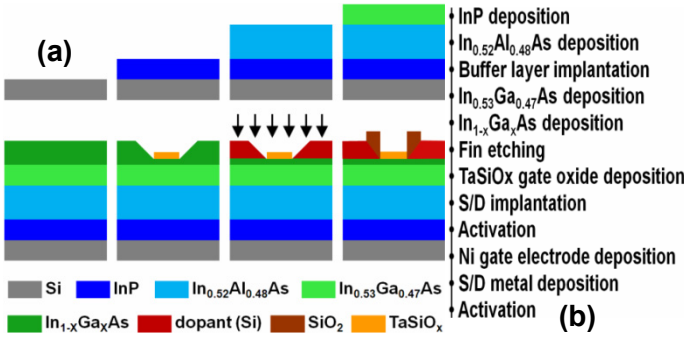
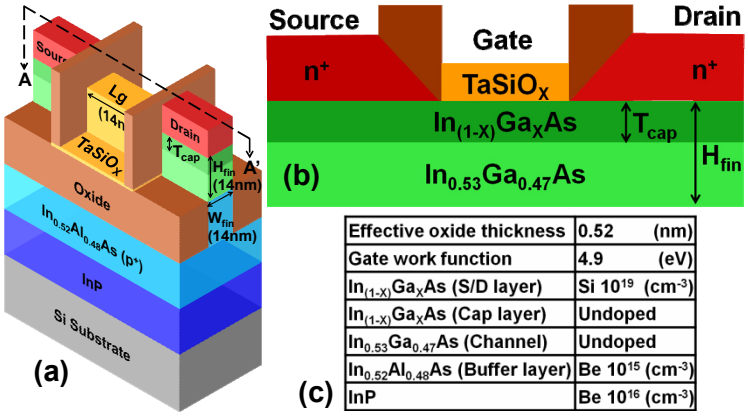


Fig. 1. (a) Illustration of the process flow of the explored device. (b) List of the fabrication steps.



Effective oxide thickness	0.52 (nm)
Gate work function	4.9 (eV)
$In_{(1-X)}Ga_XAs$ (S/D layer)	Si 10^{19} (cm^{-3})
$In_{(1-X)}Ga_XAs$ (Cap layer)	Undoped
$In_{0.53}Ga_{0.47}As$ (Channel)	Undoped
$In_{0.52}Al_{0.48}As$ (Buffer layer)	Be 10^{15} (cm^{-3})
InP	Be 10^{16} (cm^{-3})

Fig. 2. (a) 3D structure of the explored III-V trigate MOSFET. (b) Zoom-in cross-sectional view of the device, along the cutting line AA' in (a). (c) List of structural and process parameters, where T_{cap} varies from 0 to 5 nm and x is from 0.27 to 0.42, and the H_{fin} is fixed at 14 nm.

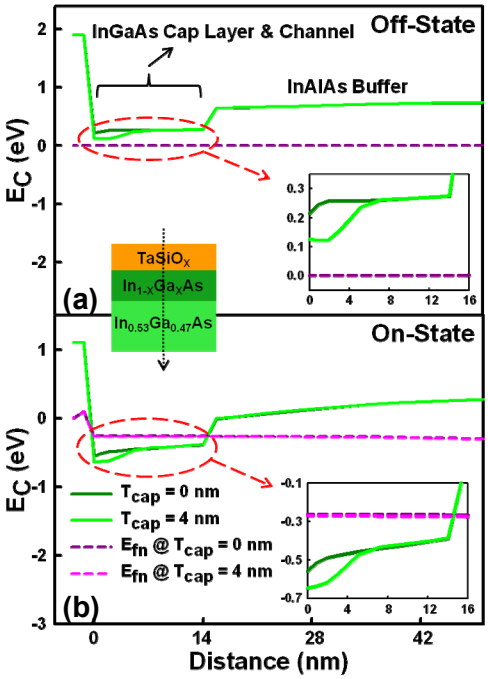


Fig. 3. (a) Off-state and (b) on-state energy band diagrams for the devices with x = 0.32 and different T_{cap} of 0 and 4 nm. The energy near the channel surface for device with 4-nm-thick capping layer is smaller than that of device without capping layer.

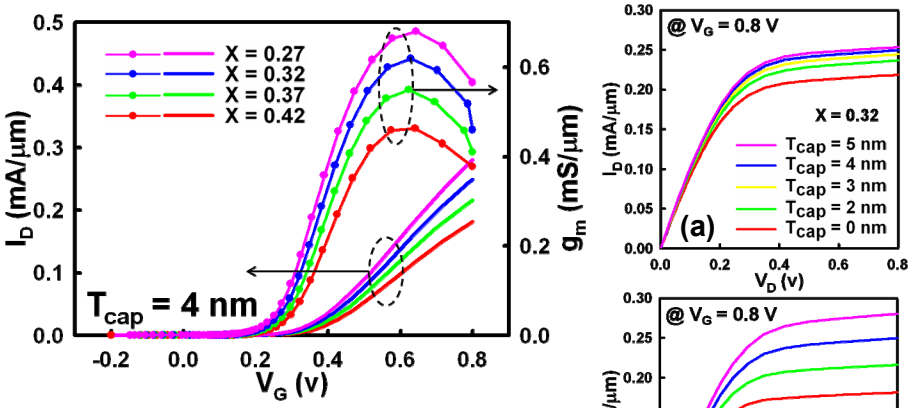


Fig. 4. Plots of I_D-V_G and g_m-V_G with different x and T_{cap} = 4 nm. A small x implies a low gallium concentration which may reduce the alloy scattering and then increase the channel mobility. Thus, it has higher drive current.

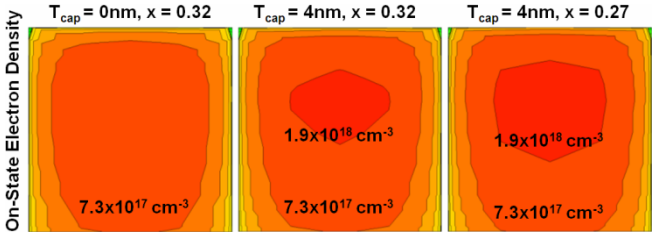


Fig. 6. The on-state electron density. T_{cap} increases or x decreases, the electron density increases and the centroid of the inversion charge density in the channel is pulled toward the gate oxide interface.

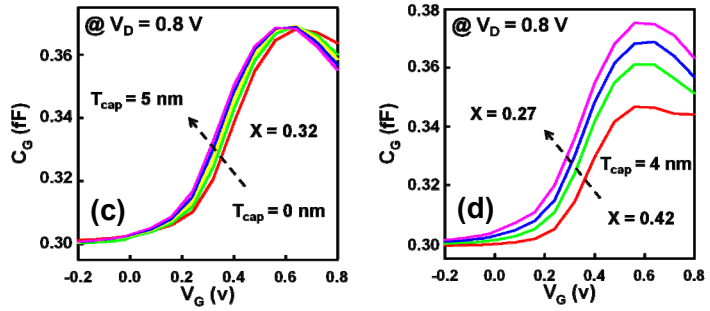


Fig. 5. (a) The I_D-V_D curves of the device with the fixed x = 0.32 and different T_{cap}. (b) The I_D-V_D curves of the device with the fixed T_{cap} = 4 nm and different x. Similar to (a) and (b), (c) and (d) are the C_G-V_G curves. We note the drain current is increased when the capping layer is increased and a small x will have large drain current. Because of the thicker capping layer and smaller band gap will result in the decrease in the S/D resistance. Both increasing T_{cap} and decreasing x enhance the gate capacitance.

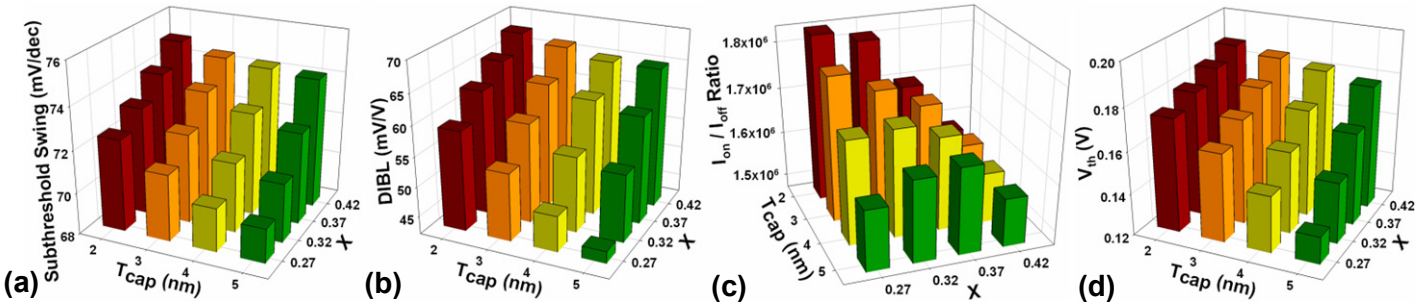


Fig. 7. Plot of (a) subthreshold swing, (b) DIBL, (c) I_{on}/I_{off} ratio, and (d) V_{th} versus the x and T_{cap}, respectively. Increasing T_{cap} and decreasing x of $In_{(1-x)}Ga_xAs$ will reduce the V_{th} and improve the subthreshold swing and DIBL; however, there is a tread-off for the variation of I_{on}/I_{off} ratio.