Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp640-641

5V High Threshold Voltage Normally-off MIS-HEMTs with Combined Partially Recessed and Multiple Fluorinated-Dielectric Layers Gate Structures

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Abstract: The combination of partial AlGaN recess etching and fluorinated multiple gate dielectric layers in MIS structure of GaN-based HEMTs is proposed and verified by both the simulation and experimental data for the first time to realize the normally-off operational mode. A high threshold voltage (V_{th}) around 5V and a low gate leakage current at pA/mm level are achieved in the fabricated MIS-HEMTs. This approach is proved to be very promising for future power electronics switching applications.

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) are emerging as promising candidates for the next-generation power electronic switching devices. Such standard AlGaN/GaN HEMTs are naturally normally-on. Normally-off operation with a large V_{th} is strongly desired in power electronic switching circuits for safety reason. Various approaches have been explored to realize the normally-off operation however with shortcomings, such as low positive V_{th}, low drain output current, and large gate leakage current. For example, deep gate recess etching of 70% AlGaN barrier thickness will lead to a severe degradation of channel conductance due to the interface scattering [1]. Fluorine ion implantation in gate barrier or single dielectric layer can shift the V_{th} to positive but it is usually not sufficiently large [2-4].

In this paper, combination of partial AlGaN recess etching and multiple gate dielectric layers with fluorination treatment for the formation of MIS structure is proposed (Fig.1). Partial AlGaN trench (~50%) using low power chlorine-based inductively coupled plasma (ICP) etching can effectively reduce 2DEG density and shift the V_{th} towards positive without obvious degradation in 2DEG channel mobility. In addition, the multiple fluorinated gate dielectric layers can further increase V_{th} to maintain normally-off mode at a higher gate voltage. The device was fabricated and the measurement data of 5V high threshold voltage further prove the feasibility of the proposal.

2. Normally-off Gate Structure and Simulations

The proposed scheme is shown in Fig. 1. Symbols "d_1"-"d_4" represent Al_2O_3 dielectric thicknesses of each layer and "d" represents the barrier recess depth. The values of d_1, d_2, and d_3 are fixed at 4nm and d_4 is fixed at 3nm in the simulation. AlGaN barrier thickness is 20nm (Al composition is 25%). The three-layer base dielectrics are employed to retain negative charges by fluorine plasma treatment at the surface of each dielectric layer. The top gate dielectric layer without any plasma treatment is used as a blocking layer to prevent the electron tunneling to reduce the gate leakage current. Partial gate trench around 10 nm (~50%) is set in the simulations.

Fig. 2 show the dependence of the device transfer characteristics when fluorination is added successively to each dielectric layer under a fixed charge density or varied within the triple fluorinated gate dielectric structure. Multiple fluorinated gate dielectric structure is found to be a very effective way to increase the V_{th} of the normally-off MIS-HEMTs. Triple fluorinated gate structure with a density of 6E12 cm^{-2} can reach a V_{th} of larger than 5 V.

3. Device Fabrication and Measurement Results

MIS-HEMTs with single gate finger and multiple fingers are fabricated. The cross-sectional schematic and the optical microscopy images are shown in Fig. 3(a) and (b) respectively. The fabrication work began with mesa isolation by selectively etching of 300 nm of the epitaxial layers. Source and drain Ohmic contacts were achieved by depositing Ti/Al/Ni/Au (25/125/45/55 nm) metals using E-beam system and annealing at 850 °C for 30 s in N_2. A 150-nm SiO_2 was deposited by PECVD for surface passivation. Then a recessed gate window with 3-μm length and 200-μm width was defined by photolithography. Gate trench of 10-nm AlGaN barrier thickness is realized by Cl^- plasma treatment in ICP-RIE system, followed by 30W RIE F^- plasma for 180s.

The innovative idea in this scheme is that low-power (30W) RIE F^- plasma treatment was implemented after each ALD-Al_2O_3 gate dielectric layer deposition. Similar processes were carried out for several rounds, followed by a good ALD-Al_2O_3 cap on the top without any plasma treatment. The total Al_2O_3 thickness is kept around 15 nm.

Fig. 4 shows the I_D-V_G transfer characteristics of the simulation and measurement data. Table I lists the F^- treatment time and employed F^-charge sheet density in the simulations. 2DEG density and electron mobility used in simulation are 8.5E12 cm^{-2} and 1550 cm^2/Vs and F^-charge

density at the AlGaN surface under the gate is 7.0E12 cm^{-2}. V_{th} values extracted on devices S-1 and S-2 from Fig. 4 are positive 2.2 and 5V. The experimental results are consistent with the simulation data. The inset of Fig. 4 shows a low gate leakage current at pA level which demonstrates the good quality of the fabricated MIS structure.

4. Conclusions

Combination of partial recess etching and multiple fluorinated MIS gate structure is proposed and verified by the simulation and experimental data for the first time to achieve the 5V high V_{th} and low gate leakage current for normally-off HEMTs.

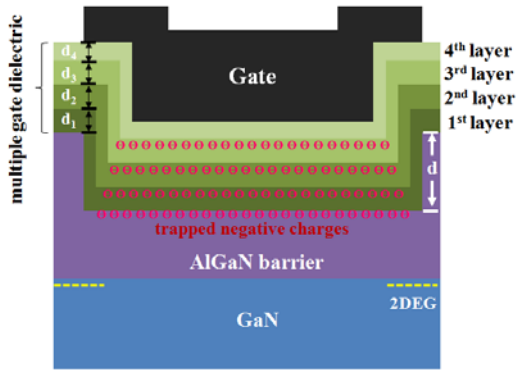

Fig. 1. Schematic of fluorinated multi-gate dielectric structure in the proposed normally-off AlGaN/GaN MIS-HEMTs.

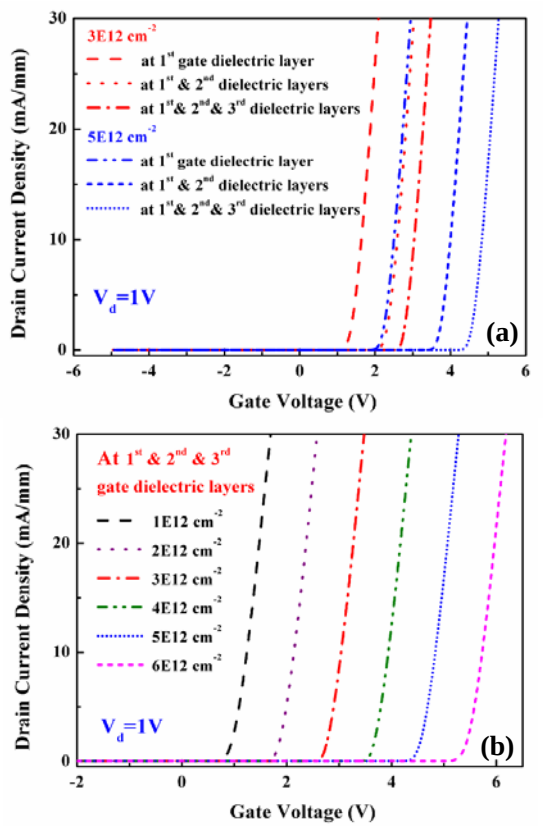

Fig. 2. Dependence of the device transfer characteristics on (a) each dielectric layer at fixed charge density and (b) the fixed negative charge density for each layer in triple fluorinated dielectrics.

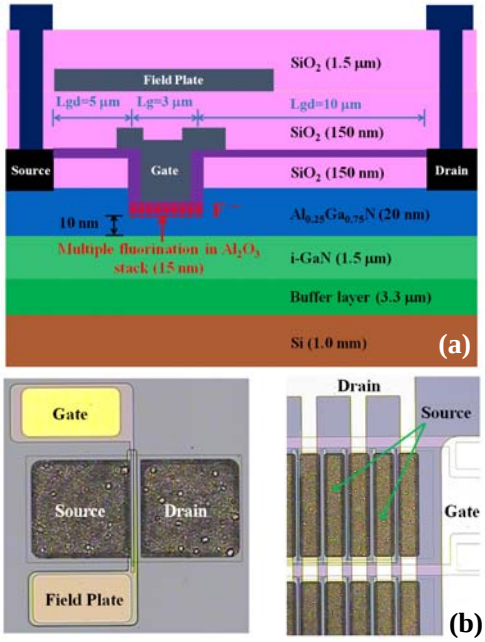

Fig. 3. (a) Device schematic and (b) optical microscopy images of the fabricated normally-off AlGaN/GaN MIS-HEMTs with single gate finger and multiple fingers.

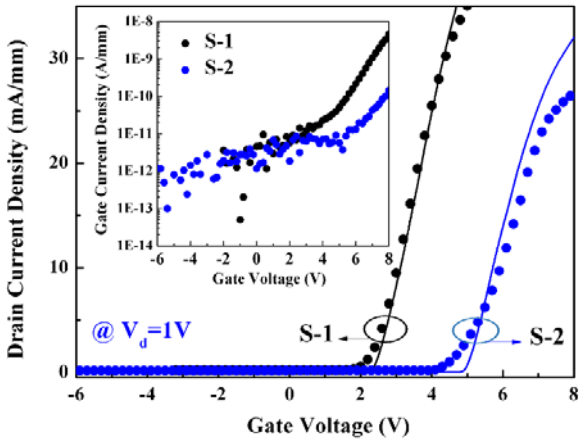

Fig. 4. Transfer characteristics of the simulation (lines) and measurement data (points) on devices S-1 and S-2. The inset shows the gate leakage current of both fabricated devices.

Table I. The F^- treatment time t_{F-} and employed F^- charge sheet density N_{F-} in the simulation in multi-gate dielectric structure

Device	1st dielectric layer		2nd dielectric layer		3rd dielectric layer	
	t_{F-}(s)	N_{F-}(cm^{-2})	t_{F-}(s)	N_{F-}(cm^{-2})	t_{F-}(s)	N_{F-}(cm^{-2})
S-1	60	3.5E12	36	2.1E12	36	2.1E12
S-2	108	5.8E12	72	3.9E12	72	3.9E12

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