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The Continuing Evolution of Silicon Carbide Power MOSFETs

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Abstract

SiC power MOSFETs are continuing to evolve in both material quality and design. Most development to date has centered on planar DMOSFETs, but trench UMOSFETs also show great promise. In this presentation we identify material and device issues limiting performance, and speculate on the path to the ultimate SiC power MOSFET.

1. Introduction

Because of its high critical field, SiC is an attractive material for the next generation of power switching devices. SiC MOSFETs have evolved along two parallel paths. The earliest power MOSFETs were trench (UMOS) designs[1], while planar (DMOS) structures appeared in 1996[2]. The latest UMOS and DMOS devices have comparable performance, but neither has reached its ultimate limits and there is considerable room for improvement, both in material quality and innovative structural geometries.

2. Planar DMOSFETs

The structure of an interdigitated power DMOSFET is shown in Fig. 1. The JFET region and current-spreading layer (CSL) have higher doping than the drift region, and the p+ base contacts are segmented along the length of the fingers (not shown)[3,4]. The specific on-resistance consists of several components, as illustrated in Fig. 2. The source, channel, JFET and substrate resistances are essentially independent of blocking voltage, while the drift region resistance increases approximately as the square of blocking voltage. Below about 2 kV, the resistance is dominated by the channel and substrate resistances, but the substrate resistance can be reduced by thinning the substrate, leaving the channel resistance as the dominant factor.

Channel resistance is proportional to channel length and inversely proportional to inversion layer mobility. Channel length is typically around 0.5 μm, limited by punchthrough considerations. The inversion layer mobility in an implanted p-well is low, in the range 15 – 30 cm^2/Vs, but can be increased by forming the channel on the A or M faces rather than the silicon face.

Reducing the cell pitch S is a major goal, but this is limited by other factors. Cell pitch is given by

$$S = L_S + L_N + L_{CH} + W_{JFET} / 2 \qquad (1)$$

Reducing source length L_S leads to increased source resistance, and an optimum is reached around 1 μm. The length L_N must provide separation between the polysilicon gate and the source ohmic contact, as well as overlap of the gate over the n+ implant.

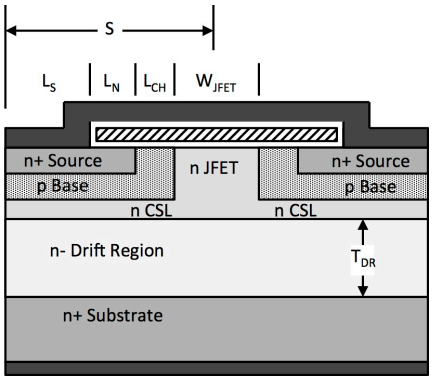

Fig. 1 Cross section of a power DMOSFET.

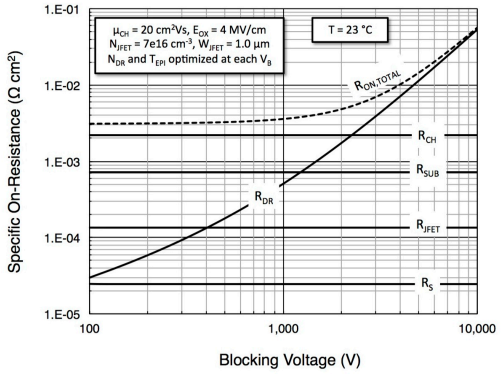

Fig. 2 Components of on-resistance in a power DMOSFET.

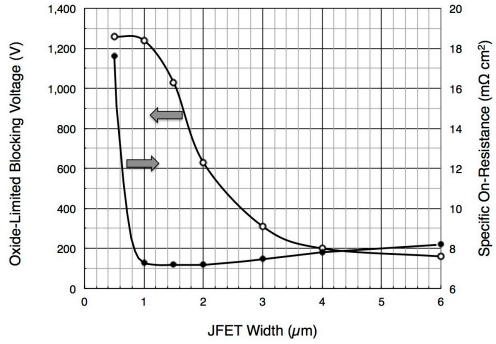

Fig. 3 Blocking voltage (as limited by the oxide field) and on-resistance as a function of JFET width in a DMOSFET.

JFET width W_{JFET} is a critical design parameter. Figure 3 shows that a small JFET width leads to a rapid rise in on-resistance, while a large JFET width reduces the shielding effect of the p base on the gate oxide in the blocking state. As W_{JFET} increases, the maximum reverse voltage must be reduced to keep the oxide field below about 4 MV/cm to insure adequate oxide reliability in operation. This is equivalent to reducing the blocking voltage. Optimizing the DMOSFET requires balancing all these factors to achieve the highest FOM, given by $V_B^2/R_{ON,SP}$.

2. Trench UMOSFETs

Figure 4 illustrates a trench UMOSFET incorporating a current-spreading layer and a p+ trench-oxide-protection (TOP) implant.[5] This implant is self-aligned to the bottom of the trench and is grounded at the end of the fingers (not shown). Without such an implant, high electric fields at the corners of the trench would lead to oxide breakdown at a low reverse voltage. The TOP implant provides the same shielding function as the p base implants in the DMOSFET of Figs. 1-3, and like the DMOSFET it creates a JFET region between itself and the p base layer. The constricting effect of the JFET is minimized by placing an n-type current-spreading layer between the base and the implant.

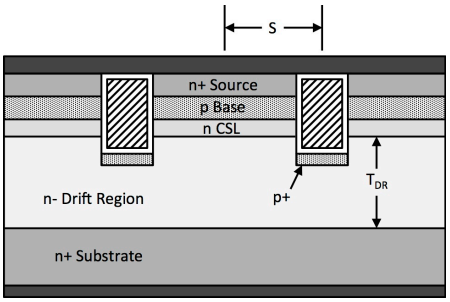

Fig. 4 Cross section of a UMOSFET with trench-oxide protection.

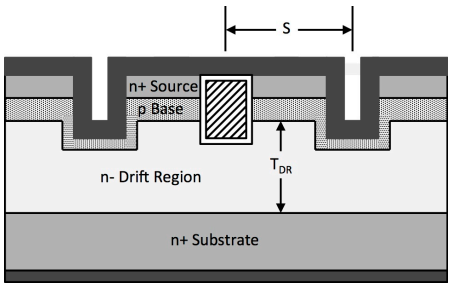

Fig. 5 Cross section of a double-trench UMOSFET.

Figure 5 shows a double-trench UMOSFET where the TOP implants are placed in inactive trenches between active MOSFET trenches.[6] With no implant under the active trench, the JFET constriction of the single-trench design is eliminated and the current-spreading layer is not needed. However, careful attention must be paid to the position of the TOP implants relative to the active trench to insure adequate shielding of the unprotected trench oxide. Moving the TOP trenches closer to the active trench improves the oxide protection, but it also reduces the source contact area, and it may reintroduce a JFET constriction in series with the current path.

3. Toward the Ultimate SiC Power MOSFET

Trench UMOSFETs offer several advantages relative to DMOSFETs. They exhibit higher inversion layer mobilities, since their channels are formed on the A face of the crystal, and they occupy less area than planar DMOSFETs. The highest $V_B^2/R_{ON,SP}$ reported to date has been achieved by UMOSFETs.[5]

The single-trench UMOSFET should have a smaller cell pitch than the double-trench structure, at the expense of increased JFET resistance. However, the double-trench design needs to demonstrate adequate shielding of the gate oxide (implying a close TOP spacing) without introducing a new JFET constriction. Consequently, the best design for the UMOSFET is still has to be decided. Other issues such as fabrication yield, cost, and long-term reliability must also be considered, and the ultimate MOSFET, whether DMOS or UMOS, is not yet apparent.

Further innovations in design are also to be expected, perhaps leading to entirely new geometries from those discussed here. Advances in oxidation technology and/or the use of deposited high-k dielectrics may increase the channel mobility, altering the trade-off between resistance components in the structure.

3. Conclusions

SiC power MOSFETs have made great progress, but the evolution is not over and the ultimate design has not yet been reached. Innovations in structure and advances in materials and processing will continue for the foreseeable future. Improved performance and reduced cost will open new markets, and increased competition will insure continued progress.

References

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