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3.3-kV Double Channel-Doped SiC Vertical JFET in Cascode Configuration

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Abstract

An SiC JFET/Si MOSFET cascode is a good solution due to high reliability, low on-resistance, high switching speed, and good gate controllability. A 3.3-kV SiC vertical JFET using a double channel-doping technique is proposed in this paper. The characteristics of a cascode including the developed JFET are also presented. A blocking voltage larger than 3.3 kV and a low on-resistance of 12.3 mΩcm^2 were achieved. Moreover, the saturation current of the cascode can be suppressed by controlling the threshold voltage of the JFET.

1. Introduction

Silicon-carbide (SiC) junction field effect transistors (JFETs) have been developed for next-generation high-power devices [1] preceding SiC MOSFETs, because they have no oxide/semiconductor interface in the channel region, which causes both gate oxide break-down and threshold voltage instability of SiC MOSFETs [2]. Given this advantageous feature of JFETs, the authors previously developed 600-V normally-off and normally-on JFETs for enhancing the current density by using the local channel doping in the p-n junction between the gate and channel regions [3, 4]. However, both normally-off and normally-on JFETs have difficulty with gate controllability, thus necessitating the need for a new gate driver circuit. In response to this need, we previously developed a normally-on SiC JFET/Si MOSFET cascode and achieved a low on-resistance and normal switching operations [4].

High voltage (> 3.3 kV) SiC transistors have been required for many applications, such as in wind power generation systems, railcars, and energy transmission and distribution systems. There have been several reports on high voltage normally-off or normally-on JFETs [5-7]. The on-resistance in these reports could not be sufficiently reduced, while high blocking voltage was achieved.

In this work, we developed a double channel doping structure consisting of an epitaxially grown channel layer and a ion-implanted local channel doping region, and designed a 3.3-kV-class low on-resistance normally-on JFET for the first time. Moreover, we assembled and evaluated a cascode with the fabricated JFET and a normally-off Si MOSFET.

2. Design of normally-on JFET

A schematic cross-sectional view of the proposed JFET structure is shown in Fig. 1. The substrate is an n-type 4H-SiC wafer containing a 30-μm-thick n-type drift layer with a doping level of 3.0 × 10^{15} cm^{-3} and a 2-μm-thick n-type channel layer with a doping level of 1.5 × 10^{16} cm^{-3}. A gate structure was formed by dry etching of the SiC epilayer and with an ion implantation of aluminum. The dry etching depth was 1.3 μm. The local channel doping regions with a doping level of 5.0 × 10^{16} cm^{-3} were formed through the ion implantation of nitrogen in some samples. The channel width, as shown in Fig. 1, is a key parameter of the JFET.

The relationships between the blocking voltage BV_{DS} and threshold voltage V_{th} of the JFETs with and without local channel-doping are shown in Fig. 2. Both the threshold voltage and blocking voltage decreased for the wider channel (lower left in the figure). The targets of the threshold voltage and blocking voltage are also shown in Fig. 2. The threshold voltage was required to be lower than -1.5 V

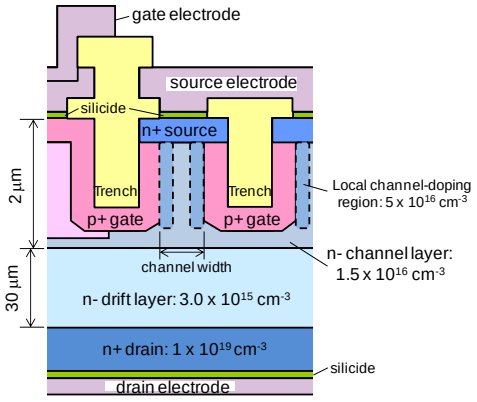

Fig. 1 Schematic cross-sectional view of proposed SiC JFET with double channel-doping.

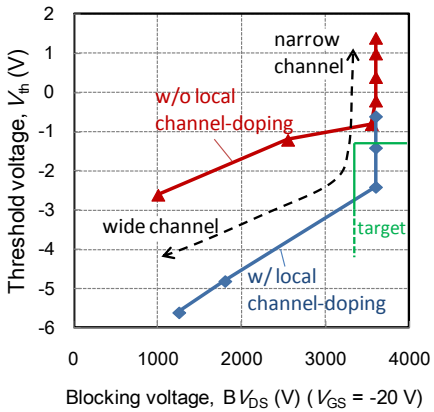

Fig. 2 Relationships between threshold voltage and blocking voltage of JFETs with and without local channel-doping.

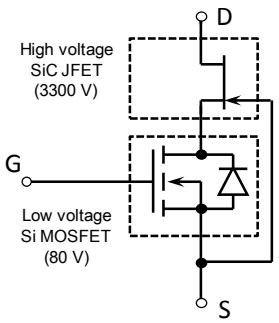

Fig. 3 Circuit diagram of cascode configuration.

for low on-resistance, since the gate voltage of the JFET in the cascode in the on-state is about 0 V. The blocking voltage decreases with the required threshold voltage without the local channel-doping. In contrast, both required blocking voltage and threshold voltage can be achieved using the local channel-doping.

A higher dopant concentration of the channel region between the p+ gate regions is required to achieve both a high blocking voltage and low threshold voltage when not using the local channel-doping. However, a higher dopant concentration of the channel layer decreases the blocking voltage in the pn junction between the p+ gate region at the bottom of the trench and the channel layer. The proposed double channel-doping structure can increase the dopant concentration only in the channel region and thus decrease the threshold voltage without degrading the blocking voltage.

3. Characteristics of cascode JFET

The fabricated 4.0-mm□ 3.3-kV SiC JFETs and 80-V, 8.4-mΩ Si MOSFETs were assembled in the cascode configuration as shown in Fig. 3. A high V_{th} (-1.4 V) JFET with narrow channels and low V_{th} (-5.4 V) JFET with wide channels were chosen for assembly and evaluation. The dependence of the drain current on the drain voltage of the cascode in the off-state is shown in Fig. 4. The blocking voltage of the high V_{th} JFET is larger than 4 kV, which is limited by the termination structure. In contrast, the blocking voltage of the low V_{th} JFET is about 3.3 kV, which is limited by the channel leakage current. In this case, the channel current can flow, although the source to gate voltage of the JFET is max (~50 V), which is limited by the reverce blocking voltage of the pn junction between the gate and the source.

The dependence of the drain current on the drain voltage of the cascode in the on-state is shown in Fig. 5. The on-resistance of the cascode with high and low V_{th} JFETs are 156 and 133 mΩ, respectively. In addition, the estimated specific on-resistance of the high and low V_{th} JFETs are 14.7 and 12.3 mΩcm^2, respectively. A lower on-resistance can be achieved using a low V_{th} JFET. On the other hand, the saturation current of a high V_{th} JFET is much smaller than that of a low one. A small saturation current is an advantage for a short circuit capability. Thus, the cascode can a achieve small saturation current with only a slight increase in on-resistance by controlling the threshold voltage of the JFET.

Finally, the dependence of the reverse drain current on the source to drain voltage is shown in Fig. 6. The reverse drain current is independent of the threshold voltage of the JFET, and the reverse offset voltage of the cascode (~0.7 V) is much lower than that of the body diode of a SiC MOSFET or a lateral channel SiC JFET (~ 2.8 V). A stand alone vertivcal JFET requires an external Schottky barrier diode (SBD) since the JFET does not have a body diode of its own. In contrast, the cascode does not require a SBD, since the reverse drain current can flow through the low on-voltage body diode of the Si MOSFET and the low on-resistance channel of the SiC JFET. As a result, the reverse offset voltage of the cascode is comparable with that of the SiC Schottky barrier diode.

4. Conclusions

We proposed a SiC vertical JFET using a double channel-doping technique. A blocking voltage larger than 3.3 kV and a low on-resistance of 12.3 mΩcm^2 were achieved. It was revealed that the saturation current can be suppressed by controlling the threshold voltage of the JFET in a cascode configuration.

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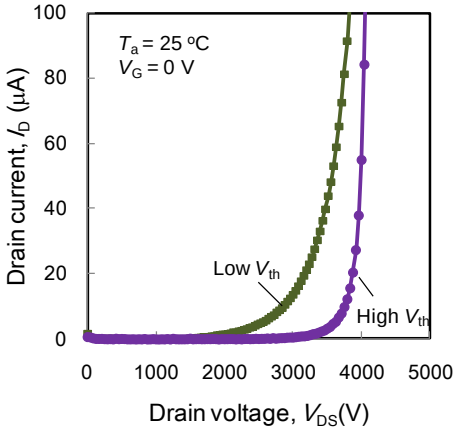

Fig. 4 Dependence of drain current on drain voltage of cascode in off-state.

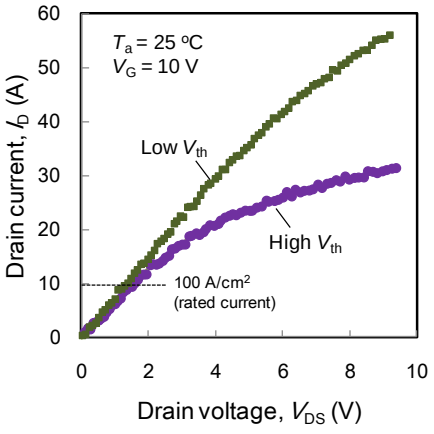

Fig. 5 Dependence of drain current on drain voltage of cascode in forward on-state.

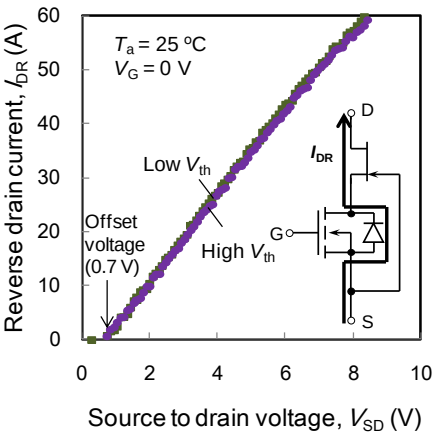

Fig. 6 Dependence of reverse drain current I_{DR} on source to drain voltage V_{SD}.