Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp648-649

High-speed and Low-leakage Characteristics of 60-nm C-axis Aligned Crystalline Oxide Semiconductor FET with GHz-ordered Cutoff Frequency

Yuto Yakubo[1], Shuhei Nagatsuka[1], Shinpei Matsuda[1], Suguru Hondo[1], Yuki Hata[1], Yutaka Okazaki[1], Yoshiaki Yamamoto[1], Masaharu Nagai[1], Shinya Sasagawa[1], Tomoaki Atsumi[1], Masayuki Sakakura[1], Toru Nakura[2], Yoshitaka Yamamoto[1] and Shunpei Yamazaki[1]

[1] Semiconductor Energy Laboratory Co., Ltd., 398 Hase, Atsugi, Kanagawa, 243-0036, Japan
Phone: +81-46-248-1131 Fax: +81-46-270-3751 E-mail: yy0934@sel.co.jp
[2]VLSI Design and Education Center (VDEC), The University of Tokyo
7-3-1 Hongo, Bunkyo-ku, Tokyo, 113-8656, Japan

Abstract

We evaluated the DC and RF characteristics of an FET using a c-axis aligned crystalline oxide semiconductor (CAAC-OS), a crystalline oxide semiconductor, with a channel length *L* of 60 nm. The CAAC-OS FET exhibits extremely low off-state leakage current, and its cutoff frequency f_T and maximum oscillation frequency f_{max} are in the order of gigahertz. Moreover, the CAAC-OS FET is applicable to a low-power large-scale integration (LSI).

1. Introduction

A c-axis aligned crystalline oxide semiconductor (CAAC-OS), a crystalline oxide semiconductor, exhibits extremely low off-state leakage current [1,2]. Here, CAAC-OS refers to indium-gallium-zinc oxide. Displays using CAAC-OS are commercially available. Furthermore, the use of CAAC-OS for CPU registers has shown reduced power consumption for large-scale integrations (LSI) [3,4]. Many studies on power reduction techniques using extremely low leakage current of CAAC-OS FETs have been reported. To extend the range of CAAC-OS applications, high-speed operation, i.e., favorable on-state as well as off-state characteristics of transistors are required.

This paper presents the high-speed characteristics of CAAC-OS FETs with a channel length *L* of 60 nm. Moreover, we fabricated a prototype of a memory circuit and measured its write time to demonstrate the applicability of CAAC-OS for LSIs.

2. Fabrication

Fig. 1 shows the main fabrication process of our CAAC-OS FET with L = 60 nm. The CAAC-OS FET has a top-gate top-contact channel-etched structure. A 15-nm-thick CAAC-OS active layer was deposited by sputtering while heating the substrate.

3. DC Characteristics

DC characteristics of a CAAC-OS FET with a total channel width W of 300 μm and a channel length L of 60 nm (i.e., 5000 CAAC-OS FETs with W/L = 60 nm/60 nm are connected in parallel) are described. Fig. 2(a) shows the drain current–gate voltage (I_d–V_g) characteristics of the CAAC-OS FET, and Fig. 2(b) shows its drain current–drain voltage (I_d–V_d) characteristics. At V_g = 2.2 V and V_d = 1.0 V, the on-state current I_{on} and the subthreshold swing are 2.87 mA and 0.09 V/dec, respectively. The off-state current is below the measurement limit, which is 10^{-13} A. This indicates that the CAAC-OS FET exhibits extremely low leakage current.

Fig. 3 shows transconductance (g_m) characteristics. The drain voltages V_d are 0.1, 1.0, 2.0, 3.0, and 4.0 V. The maximum values of g_m at V_d are 0.4, 3.9, 6.5, 8.0, and 9.3 mS when the gate voltages V_g are 1.90, 2.20, 2.35, 2.65, and 2.85 V, respectively.

4. RF Characteristics

The cutoff frequency f_T and the maximum oscillation frequency f_{max} of the CAAC-OS FET with W/L = 300 μm/60 nm (i.e., 5000 CAAC-OS FETs with W/L = 60 nm/60 nm) are derived from S parameter measurement. Fig. 4 shows the measurement results at V_d = 1.0 V and V_g = 2.2 V. We estimated f_T and f_{max} to be 1.9 GHz. We obtained these values after de-embedding using Open and Short calibration.

Fig. 5 shows the drain voltage dependence of f_T and f_{max}. In Fig. 5, f_T and f_{max} are plotted under the bias condition that g_m in Fig. 3 has the maximum value. At V_d of 0.1, 1.0, 2.0, 3.0, and 4.0 V, f_T are 0.2, 1.9, 3.4, 4.7, and 5.6 GHz, and f_{max} are 0.2, 1.9, 3.3, 4.2, and 4.8 GHz. Consequently, f_T and f_{max} increase as V_d increases.

5. Feasibility of LSI Using CAAC-OS FET

We have not observed a p-channel CAAC-OS FET that has characteristics similar to those of an n-channel CAAC-OS FET. Therefore, we fabricated a circuit composed of only n-channel FETs and a passive element to verify the operation for LSI applications. An example of such a circuit is shown in Fig. 6. We fabricated a prototype of a memory circuit and measured its write time. The memory circuit includes a transistor OS1 for writing and a transistor OS2 for reading, each of which uses a CAAC-OS FET with W/L = 60 nm/60 nm. The load capacitances C_{load} of the FETs (the sum of capacitance of a storage capacitor C_s and parasitic capacitance of interconnections) are 1.0 fF and 3.0 fF, respectively. The measurement method is as follows. First, FN voltage is set to 0.0 V by VIN = 0.0 V and VOSG = 3.0 V, then VOSG is back to −1.0 V and VIN is set to 1.1 V. After that, we input a pulse (−1.0 to 3.0 V) to a node OSG and measure the drain current of OS2. Here,

FN voltage is estimated from the I_d–V_g characteristics of OS2 which have been measured in advance. We repeat this procedure with sweeping the pulse width, and the write time is defined as the pulse width with which the FN voltage becomes 1.0 V (90% of an IN voltage of 1.1 V). Fig. 7 indicates that the write times are 4.0 ns and 2.0 ns with C_{load} of 3.0 fF and 1.0 fF, respectively.

6. Conclusion

We fabricated an FET using CAAC-OS with L = 60 nm and evaluated its DC and RF characteristics. A CAAC-OS FET with W = 300 μm exhibits an off-state leakage current of less than 10^{-13} A (the measurement limit), a subthreshold swing of 0.09 V/dec, and f_T and f_{max} of 1.9 GHz at V_g = 2.2 V and V_d = 1.0 V.

It is well known that scaling down FETs results in improved RF characteristics, which means that CAAC-OS FETs with L of less than 60 nm have higher frequencies f_T and f_{max}. This enables the CAAC-OS FETs to be used for microwave integrated circuits in the order of gigahertz.

Furthermore, we evaluated the memory write time. The write times were 4.0 ns and 2.0 ns with load capacitances of 3.0 fF and 1.0 fF, respectively. Since the CAAC-OS FET with L = 60 nm exhibits extremely low leakage current with a response speed of several nanoseconds, it is applicable to LSIs such as low-power memory.

References

[1] S. Yamazaki *et al.*, *Proc. SID'12 Dig.*, (2012) 183.

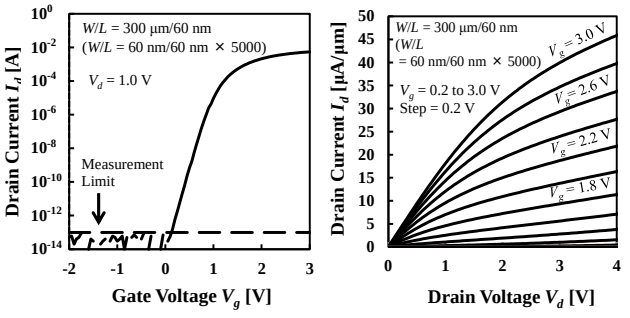
[2] K. Kato *et al.*, Jpn. J. Appl. Phys., **51** (2012) 021201.

[3] T. Ohmaru *et al.*, *Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials* (2012) 1144.

[4] K. Ohshima *et al.*, *Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials* (2013) 1100.

- Silicon wafer preparation
- Base insulator film deposition (EOT ≈ 390 nm)
- CAAC-OS film deposition (t ≈ 15 nm)
- CAAC-OS film patterning
- Source/drain electrode formation
- Gate insulator film deposition (EOT ≈ 11 nm)
- Gate electrode deposition
- Gate electrode and gate insulator film patterning
- Interconnection formation
- Passivation formation

Fig. 1 Fabrication process of CAAC-OS FET.



(a) (b)

Fig. 2 I_d–V_g characteristics (a) and I_d–V_d characteristics (b) of CAAC-OS FET with W/L = 300 μm/60 nm.

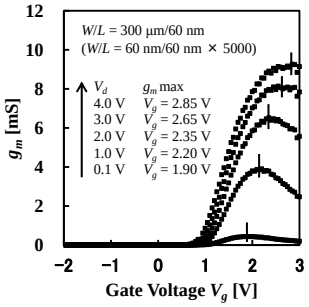


Fig. 3 g_m characteristics of CAAC-OS FET with W/L = 300 μm/60 nm.

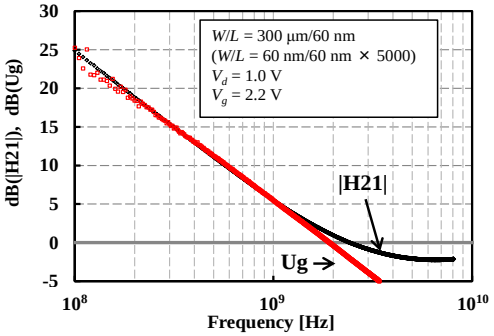


Fig. 4 RF gains vs. frequency of CAAC-OS FET with W/L = 300 μm/60 nm.

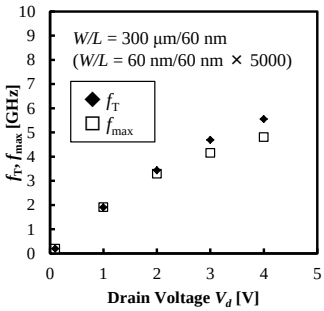


Fig. 5 f_T and f_{max} vs. V_d of CAAC-OS FET with W/L = 300 μm/60 nm.

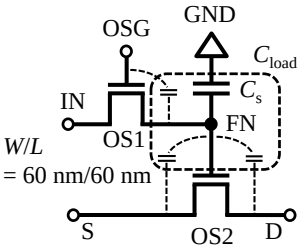


Fig. 6 Circuit for measuring memory write time.

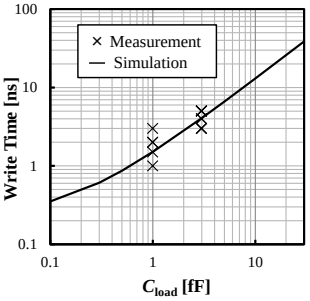


Fig. 7 Write time vs. load capacitance C_{load}.