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A Novel Method for Fabrication of Sub-100nm IGZO TFTs

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***Abstract* —IGZO TFTs were fabricated with a one-mask process method combining film-profile-engineering (FPE) concept and photoresist (PR) trimming technique. Devices with channel length of 87 nm were fabricated and characterized. Good device characteristics with steep subthreshold swing (180 mV/dec) and large on/off current ratio (>10^7) are obtained.**

1. Introduction

IGZO thin-film transistors (TFTs) have received much attention in recent years [1]–[4] in large part due to the high carrier mobility, low-temperature fabrication, and large-area uniformity. To further enhance the device performance, several studies focused on exploring devices with channel length down scaled to deep sub-micron or nanometer regimes [3]–[5]. Recently, we proposed a film-profile-engineering (FPE) approach which allows various thin films in a device to be tailored with desirable profiles. This concept has been demonstrated with the fabrication of high-performance ZnO TFTs [6][7]. In this work, the FPE concept is utilized together with photoresist (PR) trimming technique for fabrication of sub-100 nm IGZO TFTs.

2. Device fabrication

The process flow for fabricating the IGZO TFTs is shown in Fig. 1. The n^+ Si wafer was used as the bottom gate. After the deposition of sacrificial SiO_2 and poly-Si with LPCVD (step a), the source/drain (S/D) region were defined in an i-line-based photolithographic step. The PR patterns were then trimmed down in an O_2 plasma (step b). Next, poly-Si and SiO_2 were etched by reactive plasma etching and selective wet etching, respectively (step c). A suspended poly-Si bridge was formed over the substrate after the etch steps. After stripping off the PR, Al_2O_3 gate oxide was deposited by ALD (step d), followed by the deposition of an IGZO channel layer via sputtering (step e). Finally discrete S/D metal pads were formed by Al evaporation (step f).

3. Results and discussion

The perspective view of the fabricated device was shown in Fig. 2. The channel length (L) and width (W) were defined by the patterned poly-Si bridge. The cross-sectional TEM image of a fabricated device is shown in Fig. 3. As can be seen in the figure, the deposited Al S/D pads are self-aligned to the poly-Si bridge. The effective channel length (L_{EFF}) defined as the distance between the two separate Al pads is 87 nm. The transfer and output characteristics of the fabricated IGZO TFT are shown in Figs. 4(a) and 4(b). In this case, steep subthreshold swing of 180 mV/dec and large on/off current ratio of 10^7 are obtained at V_{DS}=0.1V. The field-effect mobility (μ_{FE}) is extracted to be 2.28 cm^2/V-sec at V_{DS}=0.1V. Also shown in the figures are the results of a 50 nm IGZO device reported in a previous work [4] which employed the e-beam lithography to define the channel dimensions. The major structural parameters and performance indicators extracted from the I-V characteristics of the devices are summarized and compared in Table I. From the comparison we can obviously see that our device outperform the previously reported one. One major concern associated the FPE device is the rather high off-state leakage shown in Fig. 4(a). The leakage is identified to be caused by the gate current. This is mainly attributed to the large overlap area between gate and S/D which could be improved by refining the device structure [7]. The above results evidence the feasibility of the developed FPE process for the fabrication and characterization of nanometer-scale oxide-based TFTs.

4. Conclusions

In this work, we've developed a novel method for fabricating sub-100 nm IGZO TFTs. The method incorporates the FPE concept which allows the deposited films with desirable profile and employs the PR trimming technique to shrink the channel length. Feasibility of this approach is demonstrated with the decent device performance.

Acknowledgements

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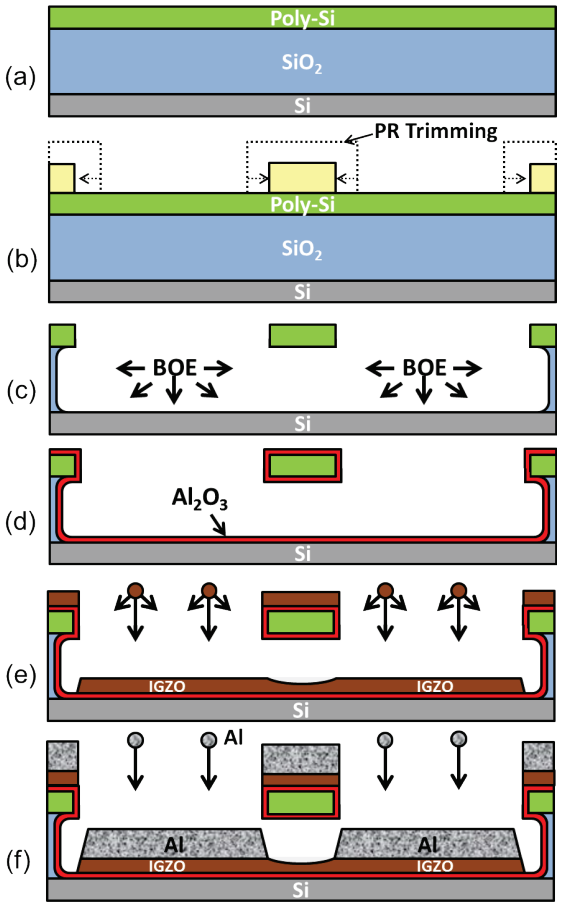

Fig. 1. Process sequence of the fabricated IGZO TFT.

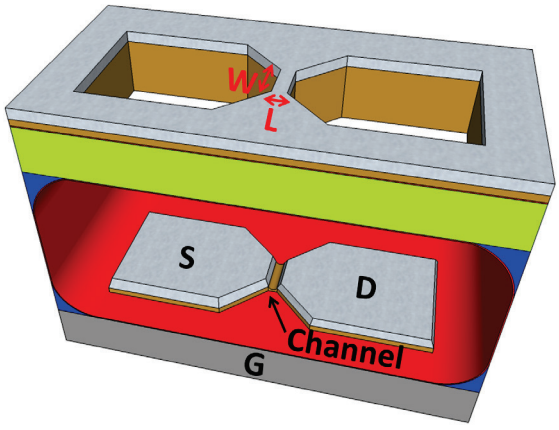

Fig. 2. The perspective view of the fabricated device. The channel length (L) and width (W) are defined by patterned poly-Si bridge.

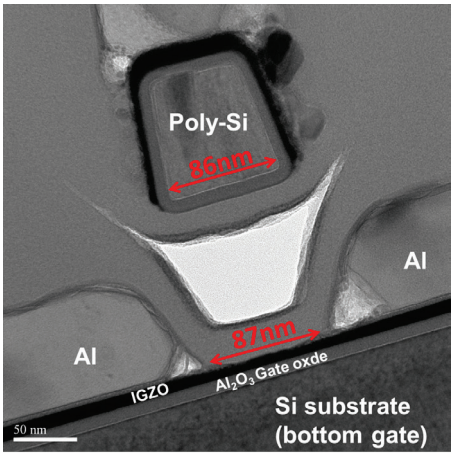

Fig. 3. TEM image of a fabricated FPE IGZO TFT with L_{EFF}=87nm.

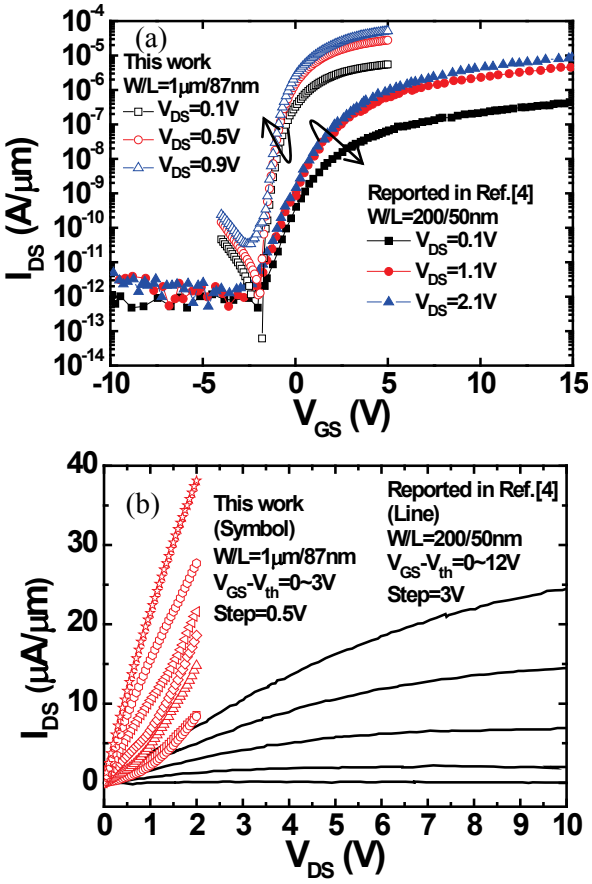

Fig. 4. Comparison of (a) transfer and (b) output characteristics of the FPE IGZO TFT with the 50 nm device reported in Ref. [4].

	This work	Previous work (Ref.[4])
Channel Length	90 nm	50 nm
Gate dielectric material (thickness)	Al_2O_3 (10 nm)	SiN (36 nm, extracted from the TEM photo)
Subthreshold Swing (V/dec)	0.18	0.684
Mobility (cm^2/V-s)	2.28	0.23
On/off current ratio	5.8×10^7 (V_{DS}=0.1V)	1.67×10^7 (V_{DS}=2.1V)
Drain current at V_{GS}-V_{th}= 3V, V_{DS}=1V	21.4 μA/μm	0.72 μA/μm

Table I. Major structural parameters and performance indicators of the FPE device and the 50 nm device reported in Ref. [4].