Fabrication of IGZO Thin-Film Transistors with Film Profile Engineering

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Abstract

IGZO thin-film transistors (TFTs) with a discrete TiN bottom gate were fabricated with film profile engineering (FPE) scheme. The fabricated devices exhibit excellent performance in terms of high on/off current ratio (>10⁶), steep subthreshold swing (91~118 mV/dec), and low leakage current. The effects of channel length on the electrical characteristics of the devices are also investigated.

1. Introduction

In the past few years, much attention has been paid on oxide-based TFTs [1][2]. For the applications in flat-panel display, some oxide semiconductors exhibit much higher mobility than that of conventional hydrogenated amorphous silicon and can meet the requirements of high-resolution displays [3]. Also, the capability of preparing thin films by sputtering tools makes oxide semiconductors compatible with the desirable low-temperature process on glass or plastic substrates. In addition to be used in display technologies, recently, an innovative concept about the integration of oxide-based TFTs into back end of line (BEOL) process of CMOS chips has been proposed and confirmed to be feasible [4]. By taking advantage of the wide bandgap of oxide semiconductors, the BEOL active devices can act as the bridging inputs/outputs between the inner low-voltage logic circuits and outer high-voltage loads. This novel idea opens up a new application area for metal-oxide semiconductors.

In the previous work, we have developed a novel film-profile engineering (FPE) method to fabricate ZnO TFTs with a common [5] or discrete bottom gate [6]. In the FPE scheme, with the aid of a suspended bridge hanging over the gate, specific deposition tools are utilized to deposit the major thin films in the device with desirable profiles. For instance, the gate oxide film prefers conformal or slightly concave profile which can be realized by using ALD or PECVD. The metal-oxide channel is suitable to be highly concave so that the amount of defects contained in the channel film at the channel center can be reduced while the effective spreading out of the current toward S/D during device operation can be retained. By controlling the deposition pressure of a sputter in the mtorr range, the highly concave metal-oxide channel can be easily obtained due to the proper scattering of the sputtered species in the chamber ambient. Finally, tools such as thermal coaters whose deposition pressure is under 10⁵ torr are appropriate to form the isolated S/D pads because the deposited species would not encounter scattering in the chamber. Thanks to the feasibility of FPE scheme, we have successfully fabricated high performance ZnO TFTs with sub-micron channel length [5][6]. In this work, we further extend this concept to fabricate and characterize IGZO TFTs.

2. Device Fabrication

The process flow for fabricating the IGZO TFTs is shown in Fig. 1. At the beginning, a TiN gate was formed on an insulator-capped Si substrate. Next, a 400nm SiO₂ and a 200nm TiN were deposited sequentially as the sacrificial layer and the hard mask, respectively. After patterning the top TiN layer by reactive ion etching, an isotropic wet etching was executed to remove the SiO₂ and after that a suspended bridge was constructed. As the bridge was formed (step 1~3), the FPE scheme (step 4~6) was performed to prepare the subsequent three films. First, a 50nm SiO₂ was deposited by PECVD, followed by a 100nm IGZO deposited by rf sputter. The isolated S/D pads were then formed by the deposition of 120nm Al using thermal coater to complete the FPE steps. Finally, a 200nm SiO₂ was capped to serve as the passivation layer and the IGZO TFTs were completed after the contact hole opening (step 7). All fabricated devices were measured by an Agilent 4156C parameter analyzer.

3. Results and Discussion

Figs. 2(a) ~ 2(c) are the transfer characteristics of fabricated IGZO TFTs measured under V_D=0.1V and 5V with channel length (L) of 0.8μm, 1μm, and 2μm, respectively. Excellent performance is obtained in terms of very high on/off current ratio (>10⁶), steep subthreshold swing (91~118 mV/dec) and low leakage current, confirming the feasibility of FPE scheme. The low leakage current is attributed to the small overlap areas between the metal gate and S/D pads and is considered to be the merit of such discrete-gate structure. Figs. 2(d) ~ 2(f) show the output characteristics of fabricated devices with L=0.8μm, 1μm and 2μm, respectively. Non-saturated characteristics can be observed in the devices with 0.8μm. This is postulated to be caused by the contact resistance between the IGZO channel and Al pads. Fig. 3(a) is the comparison of transfer curves measured at V_D=0.1V among devices with different channel length. The extracted parameters from Fig. 3(a) are shown in Fig. 3(b). The extracted field-effect mobility of fabricated IGZO TFTs is about 3~6.5 cm²/V.s. The relatively low mobility is attributed to the rough surface of the TiN gate resulted from the wet etching of the sacrificial
layer. From Figs. 3(a) and 3(b), it can be seen that the transfer curves shift positively and subthreshold swing becomes better with increasing channel length. This is due to the difference in shadowing ability among the devices with different length. As the bridge length gets longer, the shadowing effect becomes more pronounced, leading to thinner gate oxide and channel films. Therefore, devices with longer length have more positive threshold voltage and turn-on voltage.

4. Conclusion

In this work, the FPE scheme was applied to fabricate IGZO TFTs. Thanks to the small overlap between the gate and S/D, the leakage current can be significantly suppressed. The fabricated IGZO TFTs show outstanding characteristics including high on/off current ratio and good subthreshold swing. The differences in transfer characteristics among devices with different length are attributed to the distinct shadowing ability of each device.

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