Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp662-663

Body Width Dependence of Subthreshold Slope and On-Current in GaAsSb/InGaAs Double-Gate Vertical Tunnel FETs

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The dependence of subthreshold slope (SS) and on-current on the body width in a GaAsSb/InGaAs double gate vertical tunnel FET is studied through simulation and experiment. To increase the on-current, a staggered heterojunction and a narrower bandgap are effective. An increase in on-current and a steeper SS are observed when the body width is narrower and the effective oxide thickness (EOT) is thinner. When we used a 10-nm body width and a 1-nm EOT, a 16 mV/dec SS was calculated. The dependence of SS on the body width was experimentally confirmed.

1. Introduction

Recently, the performance of transistors has rapidly increased with the development of the semiconductor technology based on scaling. However, the scaling is limited by the subthreshold slope (SS) because the SS is more than 60 mV/dec at room temperature owing to the Fermi–Dirac distribution of electrons at the source. Because tunnel FETs can possibly break the limit of 60 mV/dec at room temperature, they are considered candidates for switching devices with low off-current and steep SS [1]. The problem with tunnel FETs is the low on-current due to tunneling resistance. To obtain high on-current, tunnel FETs that use a GaAsSb/InGaAs staggered (type-II) heterojunction have been studied [2].

In this work, we study the dependence of SS and on-current on the body width in a GaAsSb/InGaAs double gate vertical tunnel FET through simulation, which is then experimentally confirmed.

2. Simulation

The simulation structure is shown in Fig. 1. The model has a 40-nm-thick p^+ $GaAs_{0.51}Sb_{0.49}$ region (3×10^{19} cm^{-3}) as the source, a 40-nm-thick undoped $In_{0.53}Ga_{0.47}As$ region (5×10^{15} cm^{-3}) as the channel, and a 40-nm-thick n^+ $In_{0.53}Ga_{0.47}As$ region (1×10^{19} cm^{-3}) as the drain. The assumed carrier concentration of the p-GaAsSb layer is determined as the highest value we can achieve in fabrication. The assumed carrier concentration of the n-InGaAs layer is determined to reduce the off-current because a higher drain carrier concentration introduces a larger off-current owing to hole tunneling from the InGaAs undoped channel to the n-InGaAs drain layer. The InGaAs and GaAsSb composition is chosen as a lattice-matched composition on the InP substrate. The body width (*x*-direction, as shown in Fig. 1) is varied from 10 to 80 nm. Because we assume SiO_2 as the insulator, the insulator thickness is equal to the effective oxide thickness (EOT) and varies from 1 to 4 nm. The Silvaco Atlas simulator with a quantum module is used for the calculation. Fig. 1 shows that the axis of the conventional channel width is perpendicular to the plane (*z*-axis).

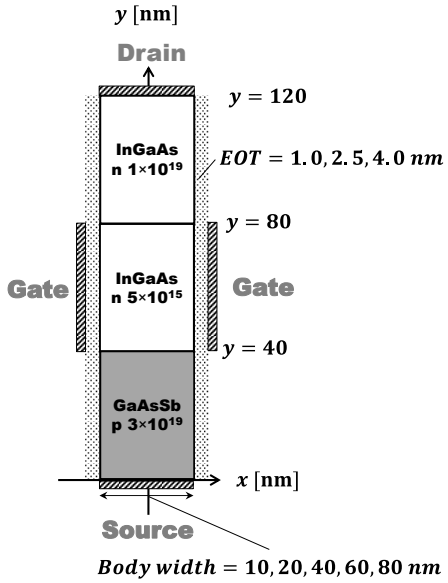

Fig. 1 Simulation structure of the tunnel FET.

Initially, to confirm the effect of the staggered heterojunction, we investigate the device with an $In_{0.53}Ga_{0.47}As$ homojunction and that with a GaAsSb/$In_{0.53}Ga_{0.47}As$ heterojunction when the EOT is 1 nm, body width is 10 nm, and drain voltage is 0.3 V [3, 4]. Unfortunately, we are unable to estimate the maximum on-current because we could not obtain convergence in the simulation when the current is more than 100 μA/μm. Thus, we evaluate the difference between the gate and threshold voltages (or the overdrive voltage) to achieve an 80 μA/μm on-current when the threshold voltage is assumed as the gate voltage for a drain current of 1 μA/μm. The required overdrive voltage of the device with the GaAsSb/$In_{0.53}Ga_{0.47}As$ heterojunction is 0.215 V, whereas that of the device with $In_{0.53}Ga_{0.47}As$ homojunction is 0.75 V. A narrower bandgap is also effective in increasing the on-current [2]. When we use the GaAsSb/$In_{0.7}Ga_{0.3}As$ heterojunction in the simulation, the required overdrive voltage is 0.12 V. On the other hand, using a narrower bandgap, the off-current changes from 7×10^{-11} to 3×10^{-8} μA/μm when we define the off-current as the minimum value. The calculated steepest SS are 23 mV/dec, 16 mV/dec, and 18 mV/dec in the

$In_{0.53}Ga_{0.47}As$ homojunction, GaAsSb/$In_{0.53}Ga_{0.47}As$ heterojunction, and GaAsSb/$In_{0.7}Ga_{0.3}As$ heterojunction, respectively.

Next, we study the dependence of the SS on the EOT and body width of the device with the GaAsSb/$In_{0.53}Ga_{0.47}As$ heterojunction, as shown in Fig. 2. The drain voltage is fixed at 0.3 V. As the EOT decreases and the body width becomes narrower, gate control is enhanced, and the SS becomes steeper. The dependence of the on-current (per channel width) on the EOT and body width is shown in Fig. 3. The on-current is defined as the current value when the gate and drain voltages are 0.3 V. We should note here that as the body width is reduced, the on-current per channel width increases, although the cross-sectional area of the channel decreases.

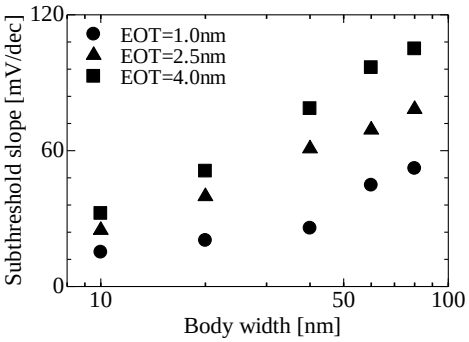

Fig. 2 Body-width dependence of the SS in the GaAsSb/$In_{0.53}Ga_{0.47}As$ heterojunction when the EOT = 1.0, 2.5, and 4.0 nm.

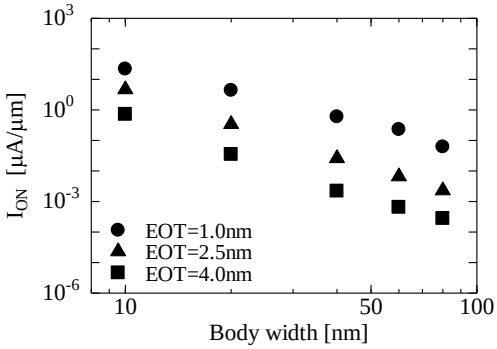

Fig. 3 Body-width dependence of the on-current in the GaAsSb /$In_{0.53}Ga_{0.47}As$ heterojunction when the EOT = 1.0, 2.5, and 4.0 nm.

To understand these characteristics, the tunneling rate of electrons and the electric concentration near the heterojunction (at y = 50 nm, as shown in Fig. 1) with body widths of 10 and 20 nm are calculated. Comparing the devices with body widths of 10 and 20 nm, the tunneling rate of electrons and the electron concentration at the center of the channel (at x = 0 nm, as shown in Fig. 1) are approximately ten times larger in the device with the 10-nm body width. Therefore, as the body width decreases, the on-current per channel width increases, although the cross-sectional area of the channel decreases.

3. Experiments

We observed the body-width dependence of devices with a GaAsSb/InGaAs heterojunction [3, 4]. We used three types of gate stacks. The first type was $In_{0.53}Ga_{0.47}As$/7.5-nm-thick Al_2O_3/Ti/Au, the second type was $In_{0.53}Ga_{0.47}As$/5.0-nm-thick Al_2O_3/Ti/Au, and the third type was $In_{0.53}Ga_{0.47}As$/5.0-nm-thick HfO_2/Al/Au. The EOTs measured by the planer MISCAP were 4.0, 3.2, and 1.6 nm, respectively. Fig. 4 shows the dependence of SS on the body width. In the devices with an EOT = 3.2 and 1.6 nm, we clearly observed the dependence on the body width. The difference between the experimental and simulated values can be explained by the interface trap density (D_{it}) [4]. The D_{it} of the $In_{0.53}Ga_{0.47}As/Al_2O_3$/Ti/Au structure was estimated as 4.2×10^{12} $eV^{-1}\cdot cm^{-2}$, and the D_{it} of the $In_{0.53}Ga_{0.47}As/HfO_2$/Al/Au structure was estimated as 2.6×10^{13} $eV^{-1}\cdot cm^{-2}$.

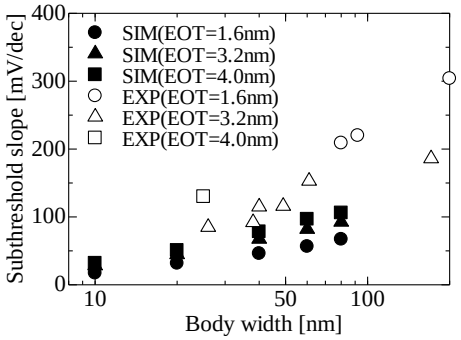

Fig. 4 Body-width dependence of SS at V_D = 0.25 V.

3. Conclusions

We have shown through simulation the dependence of SS and on-current on the EOT and body width in a double gate vertical tunnel FET based on a GaAsSb/InGaAs staggered heterojunction. To increase the on-current and make the SS steeper, a narrower body width and a thinner EOT are effective. We experimentally confirmed the dependence of the SS on the body width.

Acknowledgments

The authors would like to thank Prof. S. Arai, Prof. M. Asada, Prof. M. Watanabe, Prof. N. Nishiyama for their helpful discussions, and Dr. T. Irisawa, Dr. T. Tezuka, and Dr. M. Oda for their technical supports. This work was supported by JSPS KAKENHI Grant Number 26249046 and SCOPE by MIC.

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