Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp664-665

RF Modeling of III-V FINFETs

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Abstract

We present RF-characterization of InGaAs III-V Nanowire FinFETs, showing f_T/f_{max}=280/360 GHz. Detailed modeling taking interface traps and impact ionization into account accurately reproduce the measured data.

1. Introduction

Narrow bandgap III-V materials are promising candidates for very high performance, low power MOSFETs. This originates from the high mobility and injection velocity, which allows for very high transconductances and currents at low values of V_{DS}. There has been very strong progress, with planar In-rich FETs demonstrating g_m=2.7 mS/µm at V_{ds}=0.5 V [1].

We have recently shown selectively grown In-rich nanowire FETs demonstrating a peak g_m=2.89 mS/µm at V_{ds}=0.5 V at L_g=52 nm [2]. We here show detailed RF-studies for the FinFET, highlighting the effects due to traps and impact ionization, which both can play an important role for narrow bandgap III-V FETs.

2. General Instructions

Device Fabrication

The FinFETs studied here were fabricated on a S.I. InP substrate through a dual selective area growth process. HSQ-lines with were first formed using electron beam lithography, with a width=40 nm and spacing of 30 nm.

Using MOCVD, selective area growth of $In_{0.63}Ga_{0.37}As$ fins in between the HSQ lines with a thickness of 15 nm was performed. In this way, nanowires were formed on the surface. A second HSQ-step perpendicular to the nanowires were used as a dummy gate for selective growth of n^{++} $In_{0.53}Ga_{0.47}As$ drain/source and an InP sacrificial layer. After dummy gate removal, an Al_2O_3/HfO_2 high-k oxide was deposited, followed by a PdAu T-gate by thermal evaporation. Source/drain ohmic contacts, mesa isolation and 50 Ω GSG pads finished the processing. The device consists of 200 nanowires in parallell for a total gate width of 6.5 µm. Details of the processing can be found in ref [3].

Device Characterization

Room temperature DC measurements were first performed. The devices examined here had a peak DC g_m=1.89 mS/µm at V_{ds}=0.5 V with an R_{on}=240 Ωµm at L_g=32 nm, as shown in Fig 1. On-wafer RF measurements (100MHz-70 GHz) were performed after off-chip LRRM probe-tip calibration. The device data was deembedded through on-chip open/short structures.

RF-models

The III-V MOSFET has a small signal RF-model similar to that of a HEMT. However, III-V MOSFETs often shows an unexpected dispersion in the extracted $g_m(\omega)$ and $g_d(\omega)$. We here show that this can be explained by both border traps and impact ionization.

The effect due to border traps on the transconductance/output conductance can most easily be incorporated through a top of the barrier model. Approximating Laplace's equation through a three capacitor network C_G,C_S and C_D [4], the potential at the top of the barrier (ψ_s) in accumulation can then be written as

$$\delta\psi_s = \frac{C_G\delta V_G + C_D\delta V_D}{C_\Sigma + qD_{2D} + C_{it}(\omega)} \qquad [1]$$

where D_{2D} is the 2D density of states, and C_{it} the effect due to traps. For low frequencies, the traps can capture electrons and give rise to a substantial C_{it}. For higher frequen-

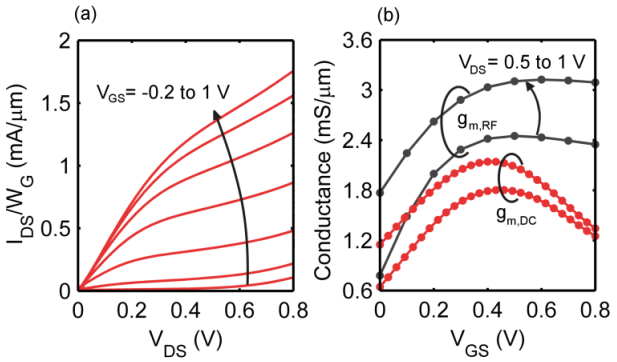

Figure 1. Output (a) and transconductance (b) data for a L_g=32 nm FinFET.

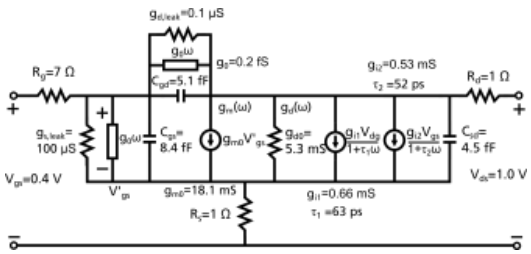

Figure 2. Small signal equivalent model.

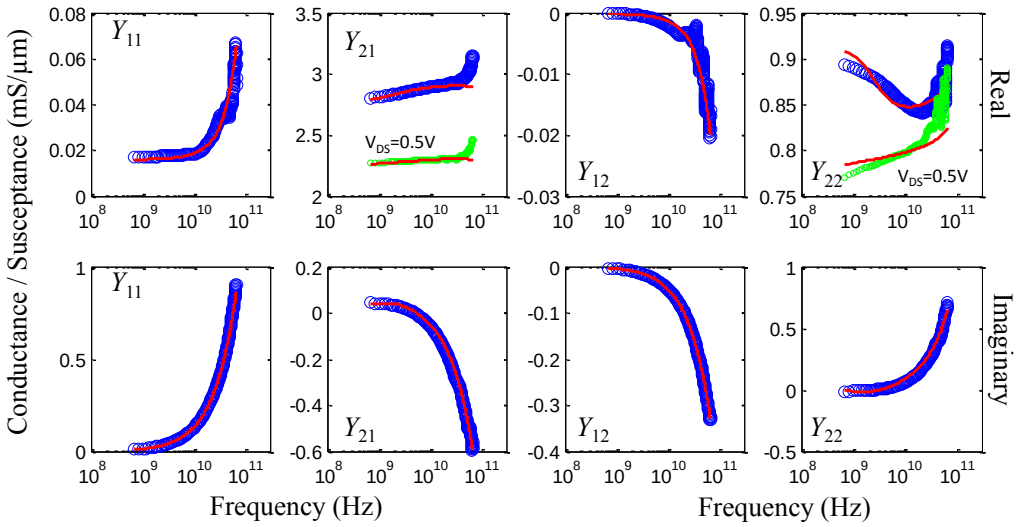

Figure 3. Measured (symbols) and modeled (solid red) y-parameters for Vds=1.0V. Re{y21,y22} also shows data for V_{DS}=0.5 V, where impact ionization is neglible.

cies, the traps cannot respond which lowers C_{it}. Since $g_d \propto \frac{\delta\psi_s}{\delta V_D}$ and $g_m \propto \frac{\delta\psi_s}{\delta V_G}$, we expect $g_d(\omega)$ and $g_m(\omega)$ to *increase* with ω in the same way. We have here modeled the traps as border traps with trapping rates limited by elastic tunneling. The real part of $\delta\psi_s$ can then be shown to be approximately $\propto (1 + \alpha \ln(\omega))$. g_m and g_d are thus expected to increase logarithmically with frequency due to the border traps.

Impact ionization can also cause frequency dispersion for both g_d and g_m. This can be modeled by adding a frequency dependent current source $\frac{g_{i1}}{1+j\omega\tau_1} V_{DG}$ between the source/drain to model the effect due to generation from a strong drain field. A second source $\frac{g_{i2}}{1+j\omega\tau_2} V_{GS}$ further models the increased impact ionization due to larger drain current. Generally, g_{i1} is a decreasing function with V_d-V_g.

For low frequencies, $y_{21} \approx g_m - g_{i1} + g_{i2}$ and $y_{22} \approx g_d + g_{i1}$.

For low values of V_{DS}≤0.5 V, there are no signs of impact ionization. The trap density is subsequently extracted from the $g_m(\omega)$ slope at low values of V_{ds}. Similar values of trap densities at V_{ds}=0.25 and 0.5 V are extracted. The trap density increases linearly with increasing V_{gs}, indicating a higher value of border traps higher in energy. The other circuit elements are then extracted using a semi-analytical approach. For larger V_{ds} where impact ionization is important, the trap density is assumed similar to that of lower values of V_{ds}. Impact ionization is clearly seen where y_{22} decreases with ω for low frequencies.

g_{i1} is first fitted from $Re(y_{22})$, and g_{i2} is then obtained from $Re(y_{21})$. In this way, excellent fits to all y-parameters can be obtained, as shown in Fig. 3. From the modeled y-parameters, the maximum f_T/f_{max} is extrapolated to 281/360 GHz respectively. These are the highest reported numbers for any III-V multi gate FET.

Interestingly, there is large discrepancy between g_{m_dc} and g_{m_RF}, as shown in Fig.1 which can be observed by comparing $Re(y_{21})$ from Fig. 3 and g_m from fig 1. We can now attribute this discrepancy as originating from a high density of border traps, in the high 10^{19} $eV^{-1}cm^{-3}$ range.

3. Conclusions

We have demonstrated RF-measurements and modeling of III-V Nanowire FinFETs. Inclusion of impact ionization and trap response is required to obtain good fits to the measured data. This illustrates the need for AC characterization when examining novel devices.

Acknowledgements

This work was supported in part by the Swedish Foundation for Strategic Research (SSF), by the Knut and Alice Wallenberg Foundation, and by the Swedish Research Council (VR).

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