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Heated Ion Implantation Technology for High Performance SOI FinFETs

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Abstract

This paper presents the impact of heated ion implantation (I/I) on SOI FinFETs performance. The defect-free extension source and drain (ESD) can be formed in ultrathin SOI layer by using heated I/I. The cap layer is essential for heated I/I to suppress the out-diffusion of the implanted ions. Heated I/I improves the I_{on}-I_{off} characteristics for both nMOS and pMOS FinFETs in comparison with conventional room temperature I/I.

1. Introduction

In sub-14nm node FinFETs, the fin channel becomes thinner than 10 nm. Thinning of the fin channel is a key technology for FinFET scaling. Furthermore, lowering of the sheet resistance (R_s) in ESD is essential for performance improvement [1]. However, in the case of conventional I/I, lowering of R_s is significantly difficult because conventional I/I generally causes poly-crystallization and/or crystal defects in ultrathin fin channel even after activation annealing [2, 3]. This problem is particularly severe for SOI FinFETs. Recently, novel I/I technology has been proposed, which is heated I/I. It has been reported that single crystallinity of the implanted layer is maintained during heated I/I, and defect free crystal can be obtained by activation annealing [4]. The I_{on}-I_{off} characteristics are improved in bulk nMOS FinFETs by heated I/I [5].

In this paper, we investigated the impact of the heated I/I technology on SOI FinFETs performance (Fig. 1).

2. Experimental

Ion implantation was performed in the hydrogen terminated Si substrate. Ion species were As^+, P^+, and BF_2^+. Implantation energy was set to 5~45 keV. Ion doses were $1.0x10^{15}$ and $1.5x10^{15}cm^{-2}$. The substrate temperature during I/I was heated at ranging from room temperature (RT) to 600°C. Subsequently, spike RTA (1015°C) was performed. The cross sectional TEM observation, the SIMS analysis, and the sheet resistance measurement were carried out.

We fabricated both nMOS and pMOS SOI FinFETs. (110) fin channel was formed on (100) SOI substrate. Doped-poly-Si/TiN/HfO_2/SiO_2 and SiO_2 gate stacks were formed and patterned. Next, ESD was formed by RT or 500°C I/I. As^+ or BF_2^+ was implanted at 5keV with total doses of $2x10^{15}cm^{-2}$. RTA was carried out at 915°C for 2sec. Finally, the back-end process was performed.

3. Results and Discussion

3.1. Crystallinity and junction depth after heated I/I

We investigated optimum implantation temperature in the heated I/I process (Fig. 2). Fig. 2(b) shows the formed amorphous layer thickness by I/I as a function of implantation temperature. The amorphous layer thickness is thinning with increasing implantation temperature. For implantation temperature higher than 400°C, the amorphous layer thickness is almost 0 nm regardless of ion species, ion doses, and implantation energy. This result means that the crystallinity is maintained during I/I, because of the dynamic annealing by the collision between the implanted dopant and Si atoms. The temperature in the implanted region gets higher by dynamic annealing. Thus, implantation temperature higher than 400°C is needed for maintaining single crystal condition.

In order to understand the crystal condition in ultrathin fin channel after heated I/I, we investigated the crystallinity of the SOI layer after RT and heated I/I using cross-sectional TEM observation (Figs. 3 and 4). I/I was performed the same condition as the ESD formation in FinFETs (Figs. 3(a) and 4(a)). In the case of RT I/I, the SOI layer is fully amorphized by I/I (Fig. 3(b)). Then, the polycrystals and twin are observed even after annealing (Fig. 3(c)). Since there are no seed crystals in SOI layer after I/I, the implanted region cannot be crystallized by activation annealing. On the other hand, in the case of heated I/I, the crystallinity is maintained in SOI layer after I/I (Fig. 4(b)). The crystal perfectly recovers by activation annealing (Fig. 4(c)). Thus, these results indicate that the defect-free ESD can be formed in ultrathin fin channel by using heated I/I.

Next, we investigated the junction depth (x_j) (Figs. 5 and 6) and the sheet resistance (Fig. 7) after heated I/I. Fig. 6 shows x_j as a function of implantation temperature. As^+ was implanted at 5 keV with doses of $1.5x10^{15}$ cm^{-2}. x_j after heated I/I slightly spreads. In the case of heated I/I, since the crystallinity is maintained during I/I, the channeling probability gets higher. This is a main reason of the spread of x_j by heated I/I. The difference in x_j before and after annealing becomes smaller with increasing implantation temperature. Fig. 7 shows the sheet resistance as a function of implantation temperature. The sheet resistance of as-implanted can be measured for implantation temperature higher than 300°C because the partial implanted dopant is activated during heated I/I. The sheet resistance after spike RTA is almost the same regardless of implantation temperature.

3.2. Importance of cap layer in heated I/I

Fig. 8 shows the retained dose ratio as a function of implantation temperature. From 400°C, the retained dose ratio decreases with increasing implantation temperature, meaning that the out-diffusion of the implanted dopant occurs during heated I/I. In the FinFETs case, since the both side of fin is open, it is concerned that out-diffusion easily occurs as compared with planar MOSFETs. Fig. 9 shows the I_{on}-I_{off} characteristics in nMOS FinFETs processed by heated I/I with and without the cap layer. In the case of no cap layer, I_{on} becomes lower and the I_{on} variation becomes large, due to the dopant loss of out-diffusion (Fig. 8). In contrast, by capping the fin, I_{on} gets higher and the I_{on} variation becomes lower. Thus, the cap layer is essential for heated I/I to suppress the out-diffusion of the implanted dopant.

3.3. Performance improvement in FinFETs by heated I/I

Fig. 10 shows the I_{on} distribution in nMOS and pMOS FinFETs proceeded by RT I/I or heated I/I with the cap layer. I_{on} in heated I/I is improved as compared with that in RT I/I regardless of nMOS and pMOS FinFETs. The resistance (R_{sd}) of ESD becomes lower in the heated I/I case (Fig. 11), due to perfect crystal recovering. This is a main reason of the I_{on} improvement by heated I/I. Furthermore, I_{off} becomes lower by using heated I/I (Fig. 12) thanks to the suppressed crystal defect formation in the channel region [6]. Thus, heated I/I is effective for improving performance in ultrathin FinFETs.

4. Conclusion

Heated I/I contributes to the formation of the defect-free ESD in ultrathin fin channel. The cap layer is essential for the heated I/I process to suppress out-diffusion during I/I. By using heated I/I, the SOI FinFETs performance is improved as compared with conventional RT I/I. Thus, heated I/I is promising as the ESD formation tool for advanced SOI FinFETs.

References

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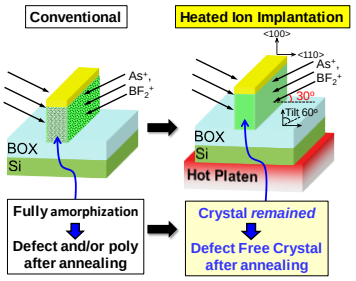

Fig. 1. Schematic illustration of conventional and heated I/I for extension S/D formation in SOI FinFETs. In the case of heated I/I, since the crystallinity is maintained during I/I, the defect-free crystal can be formed by activation annealing.

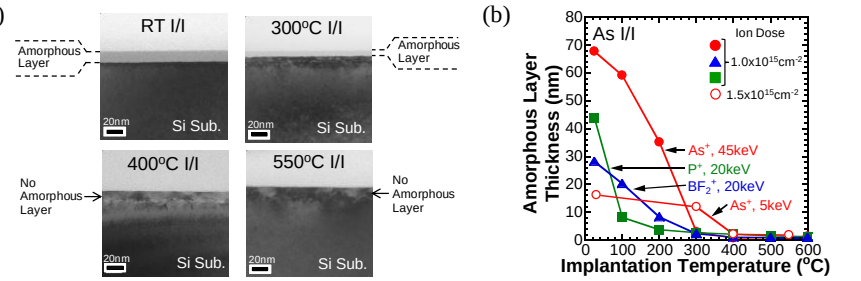

Fig. 2. (a) Cross sectional TEM images of Si substrate after RT, 300°C, 400°C, and 550°C I/I. As^+ was implanted at 5keV with doses of $1.5x10^{15}$ cm^{-2}. (b) Formed amorphous layer thickness by I/I as a function of implantation temperature. (a) In the case of RT I/I, the amorphous layer is observed. For implantation temperature higher than 400°C, the crystallinity is maintained. (b) The amorphous layer thickness decreases with increasing implantation temperature and becomes almost 0 nm for implantation temperature higher than 400°C regardless of ion species, implantation energy, and ion doses.

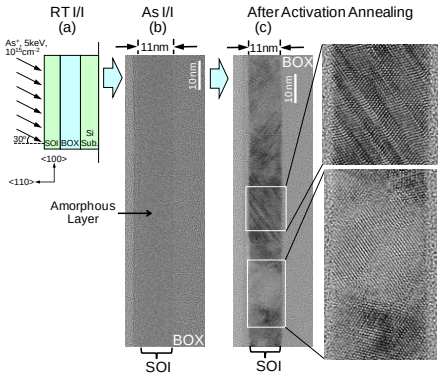

Fig. 3. (a) Schematic illustration of RT I/I in ultrathin SOI layer. (b) and (c) cross sectional TEM images of 11-nm-thick SOI layer after RT I/I and annealing. (a) The I/I conditions were set to the same condition as the ESD formation in FinFETs. (b) The SOI layer is fully amorphized. (c) The polycrystal and twin are observed.

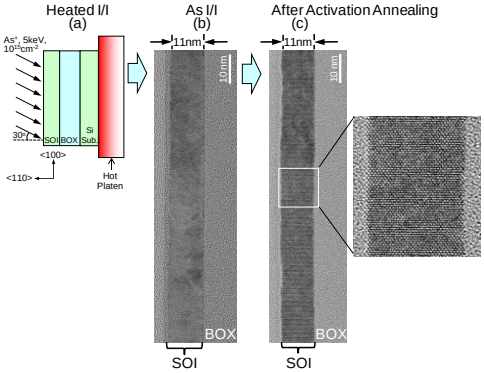

Fig. 4. (a) Schematic illustration of heated I/I in ultrathin SOI layer. (b) and (c) cross sectional TEM images of 11-nm-thick SOI layer after heated I/I and annealing. (b) All SOI layer is maintained the crystal condition. (c) The SOI layer is perfectly crystallized by annealing.

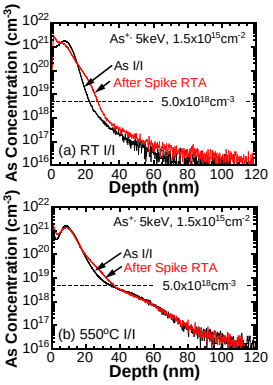

Fig. 5. Arsenic concentration as a function of depth in (a) RT and (b) 550°C I/I.

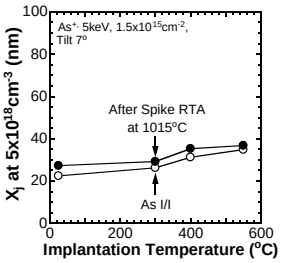

Fig. 6. Junction depth (x_j) as a function of implantation temperature. The difference in x_j before and after annealing becomes smaller with increasing implantation temperature.

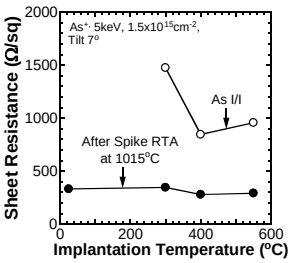

Fig. 7. Sheet resistance as a function of implantation temperature. The sheet resistance of as-implanted can be measured for implantation temperature higher than 300°C.

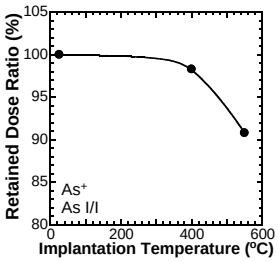

Fig. 8. Retained dose ratio as a function of implantation temperature. From 400°C, the retained dose ratio decreases with increasing implantation temperature, which means that out-diffusion arises during I/I.

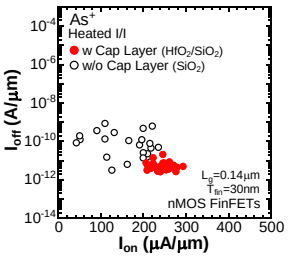

Fig. 9. I_{on}-I_{off} characteristics in nMOS FinFETs proceeded by heated I/I with and without cap layer. In the case of no cap layer, I_{on} is lowered and the I_{on} variation becomes large. In contrast, by capping the fin, I_{on} gets higher and the I_{on} variation becomes lower.

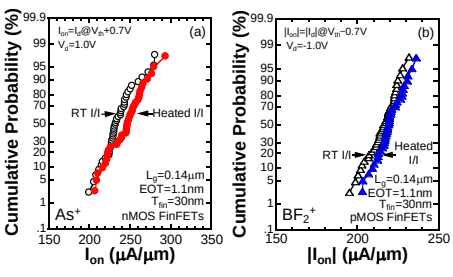

Fig. 10. I_{on} distribution in (a) nMOS and (b) pMOS FinFETs proceeded by RT I/I or heated I/I with cap layer. I_{on} in heated I/I is improved as compared with that in RT I/I.

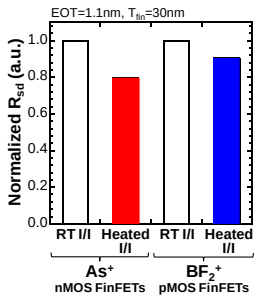

Fig. 11. Normalized R_{sd} in nMOS and pMOS FinFETs. The normalized R_{sd} in heated I/I is improved as compared with the RT I/I case.

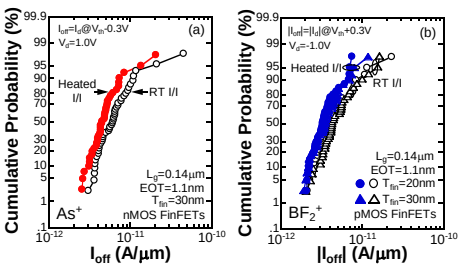

Fig. 12. I_{off} distribution in (a) nMOS and (b) pMOS FinFETs proceeded by RT I/I or heated I/I with cap layer. I_{off} in heated I/I becomes lower as compared with that in RT I/I regardless of nMOS and pMOS FinFETs.