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Operations of CMOS Inverter and Ring Oscillator Composed of Ultra-Thin Body Poly-Ge *p*- and *n*-MISFETs for Stacked Channel 3D-IC

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Abstract

Poly-Ge CMOS inverter and ring oscillator have been successfully fabricated and demonstrated for the first time. Ultra-thin body poly-Ge *p*- and *n*-MISFETs are fabricated on 10nm-thick planar poly-Ge channel layer which is deposited by sputtering and crystallized by lamp annealing at high temperature. Low I_{off} due to depletion-type channel and appropriate V_{th} in CMOS due to Si cap lead to poly-Ge IC operations.

1. Introduction

Sequential integration by stacking channel materials such as poly-Si [1], poly-Ge [2-5] or oxide semiconductors [6, 7] has been investigated for future three dimensional (3D) IC [8]. Poly-Ge is one of the attractive materials due to higher μ and lower poly-crystallization (PC) temperature compared to poly-Si. Since both *n*-FETs and *p*-FETs can be fabricated on the same poly-Ge layer [4, 5], poly-Ge channel is preferable for the cost-effective manufacturing compared to dual oxide channels [7]. Although main drawbacks of Ge channel such as large GIDL and DIBL originating in small E_g and large ε can be overcome by using depletion-type, or junctionless (JL), tri-gate *p*- and *n*-FETs in which the fin channel width was as narrow as around 10nm [3-5], planar channel is desirable compared to the fin one in terms of the cost. Although poly-Ge fin-channel *p*-FETs and *n*-FETs [4, 5] have recently been reported, operation of CMOS circuits composed of poly-Ge *p*- and *n*-FETs has not been reported so far. Threshold voltage (V_{th}) control of the FETs and improving crystal quality of the poly-Ge layer would be keys to realizing the circuit operation. Recently, we have demonstrated threshold-voltage control for both *p*- and *n*-JL-FETs by using a thin Si capping layer on a poly-Ge channel [4]. A high-temperature annealing at temperatures near or over the melting point of the initial amorphous Ge layer is a possible solution to improve the crystal quality [5]. A laser annealing (LA) process for PC is a practical process to avoid thermal degradation of ICs under the layer. In this study, we investigated process conditions to make the ultra-thin body (UTB) poly-Ge layer using a conventional lamp annealing instead of the LA process to clarify the temperature. Operations of poly-Ge CMOS inverter and ring oscillator which are the fundamental components in 3D-IC were demonstrated for the first time by using an appropriate annealing condition, a depletion-type FETs and a V_{th} control with Si capping.

2. Device fabrication

Key fabrication steps of UTB top gate poly-Ge *p*- and *n*-FETs are summarized in Fig. 1. Lamp annealing was used for PC of amorphous Ge layer which is deposited by sputtering. In order to reduce parasitic resistance (R_{para}) at source/drain regions, self-aligned nickel germanidation was employed [3]. There was no doping for *p*-FET, whereas phosphorous was doped in *n*-FET.

3. Results & discussion

UTB poly-Ge p-&n-MISFETs

Firstly, we compared I_{on}/I_{off} ratio of *p*-FETs in the case of poly-Ge thickness (t_{Ge}) of 16nm and 10nm which were fabricated by annealing at 860 and 840°C, respectively (Fig. 2). Although a large I_{on} was obtained in the 16nm thick *p*-FET, thinner Ge of 10nm is better to obtain higher I_{on}/I_{off} due to small I_{off}. Moreover, since a large I_{off} results in a large penetration current in CMOS IC which is undesirable for low power operation, thinner t_{Ge} of 10nm is better for the following feasibility study of poly-Ge IC. The typical grain size in the 10nm-thick poly-Ge layer was 10~30nm as shown in TEM images (Fig. 3). The average grain size estimated from Raman spectra in Fig. 4 increased with the increase in annealing temperature. The increase in grain size can lead to high μ. Since the average grain size of the sample after phosphorous ion implantation (I/I) followed by activation annealing (AA) was almost the same as that before P I/I and AA, a degradation of I_{on} in *n*-FET compared to that in *p*-FET can be expected as small. Figs. 5 and 6 show that poly-Ge *n*-FET as well as *p*-FET has been successfully fabricated and demonstrated, even though channel-type and gate-electrode was planar-type and top-single-gate, respectively. Annealing at high temperature is a key to obtaining good FET characteristics. Since *p*-FET in Fig. 5(a) was normally-on, negative fix charge for positive V_{th} shift in both *p*- and *n*-FETs can emerge at the BOX/poly-Ge interface at high temperature annealing process. Since V_{th} difference between *p*- and *n*-FETs was 1.2V which is comparable to the reported one [4], Si cap was still effective toward depleting the channel surface in both *p*- and *n*-FETs in this study. Fig. 7 shows that carrier concentration (N_C) decreased with the increase of annealing temperature and the tendency was independent of poly-Ge thickness. Moreover, thicker t_{Ge} of 16nm was more effective for obtaining higher μ than t_{Ge} of 10nm. The reason for μ independent of annealing temperature in 10nm-thick poly-Ge layer may relate to surface depletion due to the fixed charge at the BOX/poly-Ge interface. The LA process is adaptable for UTB poly-Ge of around 16nm which can satisfy both high μ and low N_C for improving poly-Ge FET characteristics by introducing high energy density at the surface which corresponds to high temperature annealing in this study.

Poly-Ge CMOS inverter & ring oscillator

The successful inverter operation with reasonable gain was observed, which is the first demonstration of poly-Ge CMOS circuits (Fig. 8). Moreover, forty one stages ring oscillation has been demonstrated for the first time (Fig. 9). Low I_{off} due to depletion-type channel [3, 4] and appropriate V_{th} in CMOS due to Si cap [4] led to poly-Ge IC operations. It should be noted that ring oscillation as well as CMOS inverter operation using single-crystalline Ge CMOS has never been reported.

4. Conclusions

UTB poly-Ge *p*- and *n*-MISFETs were fabricated on planar poly-Ge layer of 10nm. Poly-Ge CMOS inverter and ring oscillator have been successfully fabricated and demonstrated for the first time. These results will pave the way for the monolithic integration of poly-Ge CMOS in 3D-IC.

Acknowledgement

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References

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- Ge deposition on SiO_2/Si substrate by sputtering
- Active area formation
- Poly crystallization by lamp annealing at high temperature
- Lithography process for *n*-FETs region (N), phosphorus I/I and activation annealing
- Gate stack (TaN/HfAlO/SiO_2/Si on poly-Ge) formation
- Self-aligned NiGe layer formation
- BEOL process (1M)

Fig. 1 Fabrication process flow for poly-Ge CMOS circuits.

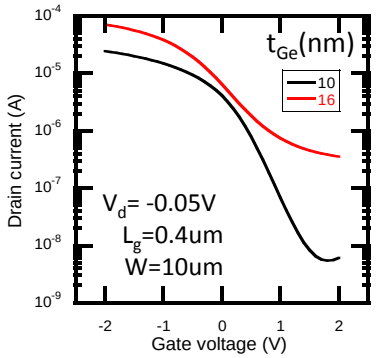


Fig. 2 Comparison of I_d-V_g curves between t_{Ge} of 10nm and 16nm.

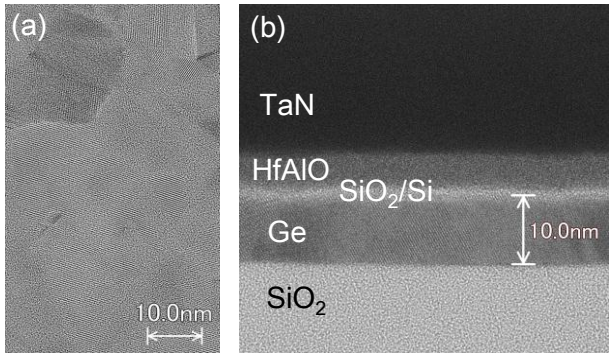
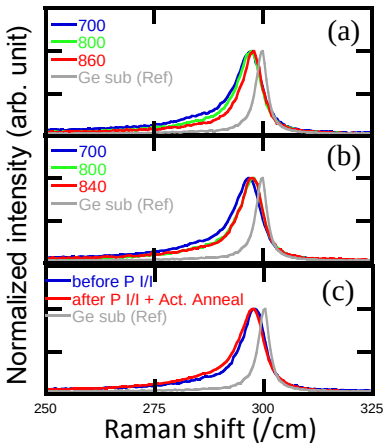


Fig. 3 (a) Plane-view and (b) cross-sectional TEM images of 10nm-thick poly-Ge layer.



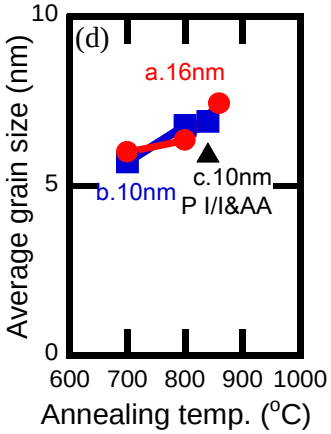


Fig. 4 Normalized Raman spectrum in poly-Ge of (a) 16nm, (b) 10nm, and (c) 10nm with or without P I/I & AA where annealing temperature is a parameter in (a) and (b). (d) Corresponding grain size estimated from (a) to (c) [9]. The decrease in the spectra at small Raman shift region means the decrease in an amount of small grain.

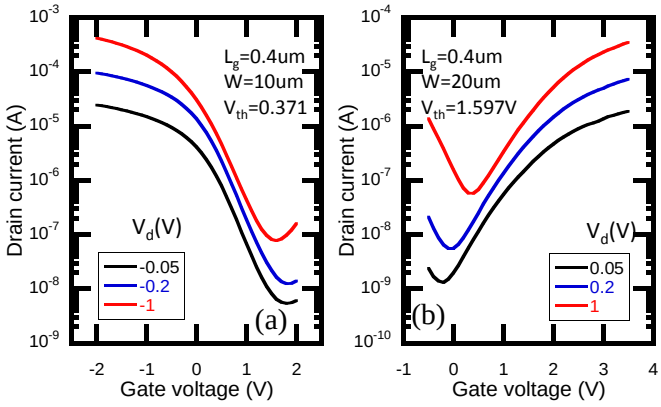


Fig. 5 I_d-V_g curves of (a) *p*-FET, and (b) *n*-FET. ΔV_{th}(=$V_{th,n}$-$V_{th,p}$=1.226V) is comparable to the reported value of 1.293V in the Si caped JL *p*- and *n*-FETs [4].

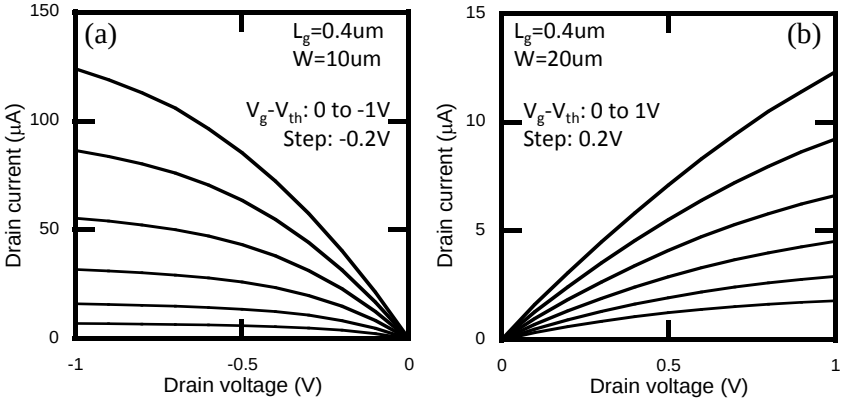


Fig. 6 I_d-V_d curves of (a) *p*-FET, and (b) *n*-FET.

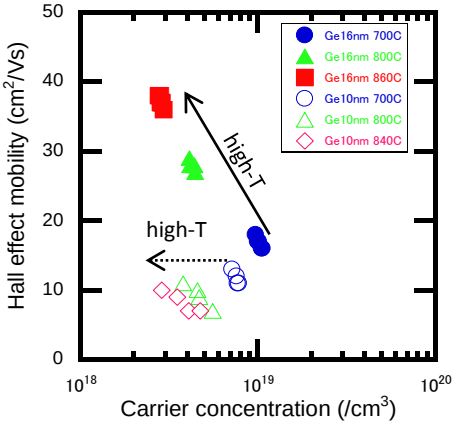


Fig. 7 Hall effect mobility of 10 and 16nm-thick poly-Ge layer after annealing as a function of carrier concentration (N_C) where annealing temperature is a parameter.

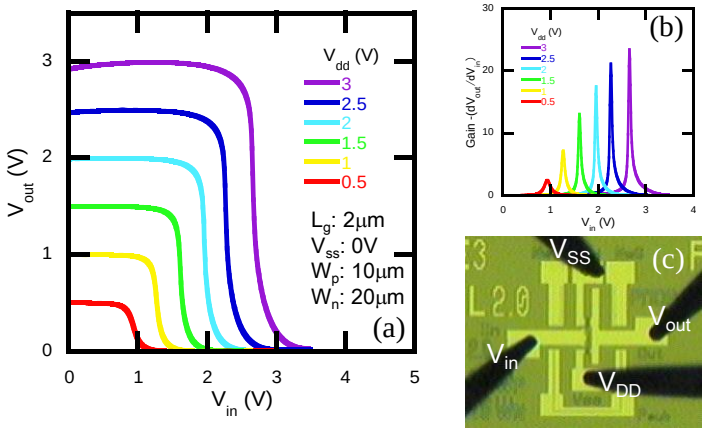
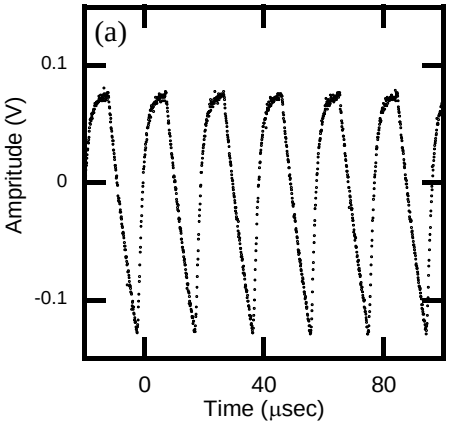
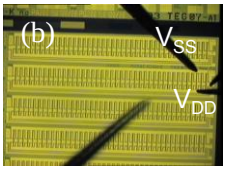


Fig. 8 (a) Voltage transfer characteristics and (b) corresponding voltage gain of poly-Ge CMOS inverter where V_{dd} is a parameter. (c) Photo image of poly-Ge CMOS inverter.





Stage: 41
L_g: 2μm
W_p: 40μm
W_n: 100μm
V_{dd}: 2.3V
V_{ss}: 0V
Frequency: 52kHz

Fig. 9 (a) Ring oscillation composed of 41 stages measured at AC mode. Inverter ring frequency is 52kHz at V_{dd} of 2.3V. (b) Photo image of poly-Ge CMOS ring oscillator.