Extended Abstracts of the 2014 International Conference on Solid State Devices and Materials, Tsukuba, 2014, pp670-671

Atomically Flattening of Si Surface of SOI and Isolation-patterned Wafers

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Abstract

By introducing high-purity low temperature Ar annealing at 850°C, atomically flat Si surfaces of SOI and STI-patterned wafers were obtained. Gate oxide reliability of STI-patterned MOS capacitor was improved due to atomically flat Si/oxide interface.

1. Introduction

Atomically flattening of semiconductor/gate insulator interface has received much attention for improving gate insulator reliability and field effect mobility of CMOS devices [1-3]. Atomically flat Si surface having atomic terraces and steps is known to be obtained by Ar or Ar/H_2 annealing at temperature of 1100 ºC or higher [4]. By reducing the concentrations of H_2O and O_2 residue gases down to less than 30 ppb, the flattening temperature was able to be decreased to 850 ºC [5]. In this work, in order to evaluate the applicability of this technology to scaled-down CMOS LSI process, Si surface flattening effect is measured for SOI and isolation-patterned wafers. The low process temperature is to be essential to suppress a reaction of SiO_2 and Si where they coexist in these wafers.

2. Experimental

(100) oriented Si substrates with three structures were employed in this study as shown in Figs. 1(a)-1(c), i.e., (a) SOI wafer (blank), (b) Si substrate having isolated patterns of field oxide film and (c) Si substrate having shallow trench isolation (STI) patterns. Process flows of these structures are also described in the figure. In the field-oxide case, two kinds of Si dioxide films, NSG film by 400 ºC APCVD and thermal SiO_2, were employed. Ar annealing for atomically flattening was carried out using an ultra-clean annealing furnace. H_2O and O_2 residue gas concentrations are less than 30 ppb in the process ambient [5].

2. Results and Discussions

A. SOI wafer

The effects of concentrations of H_2O and O_2 to surface reactions of Si-wafer during annealing at various temperatures have been previously investigated, as shown in Figs. 2(a) and 2(b) [6-7]. The results indicate that reduction of H_2O and O_2 concentrations in ambience is essential to obtain atomically flat Si surface especially at low temperature. Figs. 3(a) and 3(b) show AFM images of surface of 200-mm-diameter SOI wafer (wafer center region) after Ar annealing at 850ºC for 3 hours and (b) thicknesses of SOI layer of the various regions of wafer as a function of annealing temperatures of 850ºC and 1200ºC. Atomically flat surface of SOI layer was obtained by low temperature Ar annealing (850ºC). In the case of 1200ºC Ar annealing, SOI layer was completely vanished, suggesting that Si of SOI layer was evaporated due to the reaction with oxygen of buried oxide layer.

B. Field-Oxide-Isolated Patterns

Figs. 4(a) and 4(b) show AFM images of the active region of field-oxide isolated patterns of (a) before (initial condition) and (b) after Ar annealing at 900 ºC (1 hour) in the case of thermal-SiO_2 field oxide. The atomically flat surface was obtained. On the other hand, Figs. 4(c) and 4(d) show AFM images of the active region after Ar annealing at (c) 850 ºC (3 hours) and (d) 900 ºC (3 hours) in the case of NSG field oxide. Atomically flat surface was not obtained for both temperature cases. Fig. 4(e) shows bare Si wafer surface without isolation-pattern after Ar annealing at 900 ºC (1 hour) with intentionally-added 20-ppm O_2, showing that surface structure was similar to those in Figs. 4(c) and 4(d). Figs. 5(a) and 5(b) show SEM images of NSG field-oxide film at the edge of active region (a) before and (b) after Ar annealing at 900ºC (1 hour), and Fig. 5(c) shows enlarged image of Fig. 5(b) obtained by TEM. It was found from SEM images that the NSG film shrank due to the Ar annealing. The results suggested that oxygen is emitted from the NSG film, and the oxygen reacted with Si. Also, as shown in TEM images in Fig. 5(c), shape anomaly at the edge of active region was observed. This may be resulting from both reduction action of NSG and migration of Si at the edge. The results suggest that lowering of annealing temperature to suppress such reactions is critical when oxygen and Si coexist in a target wafer. In addition, a quality of SiO_2 film also affects the Si flattening result, i.e., SiO_2 films with higher density may be necessary to obtain an atomically flat Si surface as it suppresses oxygen emission and keep an oxygen concentration low in the annealing ambience.

C. STI patterns

Figs. 6(a) and 6(b) shows AFM images of the active region (p-well) of STI pattern after Ar annealing at (a) 850 ºC (5 hours) and (b) 900 ºC (6 hours). Atomically flat Si surface was successfully obtained for 850 ºC. On the other hand, that could not be obtained for 900 ºC and surface structure was similar to those in Fig. 4(c)-4(e) suggesting that oxygen was emitted from SiO_2 film. Figs. 7(a)-7 (c) shows the gate current as a function of electric field applied to the gate oxide film and distribution of oxide breakdown electric field. Here, the gate oxide film was formed by oxygen radical oxidation which can preserve an atomic flatness at the Si/oxide interface [8]. An improvement of gate-oxide reliability was obtained by atomically flattening of Si surface having STI pattern.

3. Conclusions

The developed high purity Ar annealing at 850 ºC for Si atomically flattening is shown to be applicable to SOI and STI-patterned wafers. The atomically flattening process is to be easily installed to existing CMOS manufacturing process flow for the improvements of semiconductor/gate insulator interface quality of both SOI and bulk devices.

Acknowledgements

This work was supported partly by JSPS KAKENHI Grant Numbers 22000010 and 24360129.

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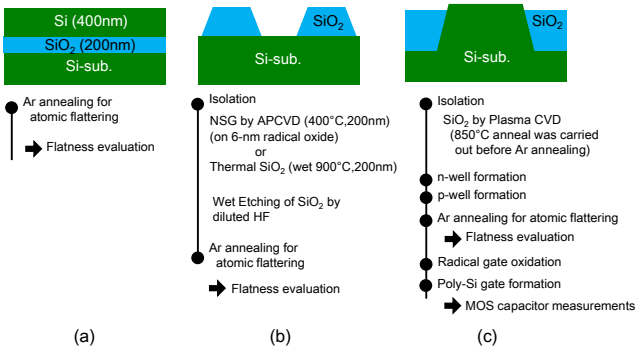

Fig. 1 Structures investigated for atomically flattering in this study: (a) SOI wafer, (b) field-isolated pattern by NSG (200 nm)/radical oxide(6 nm) films and (c) STI pattern with plasma CVD SiO_2 film annealed at 1100ºC.

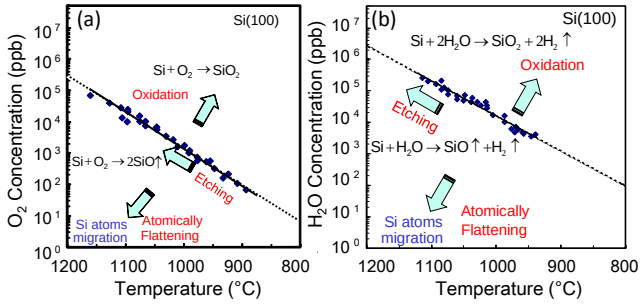

Fig. 2 Effects of concentrations of (a) H_2O and (b) O_2 to surface reactions of Si-wafer during annealing at various temperatures [6-7].

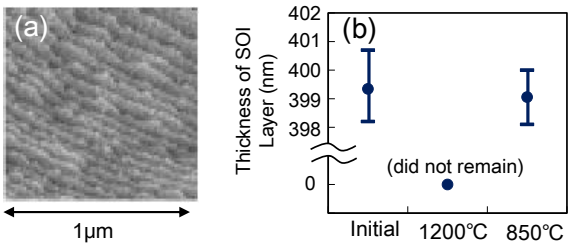

Fig. 3 (a) AFM images of surface of 200 mm SOI wafer after Ar annealing at 850ºC for 3 hours (wafer center). Atomically flat Si surface was successfully obtained. (b) Thicknesses of SOI layer of the various regions of wafer as a function of annealing temperatures of 850ºC and 1200ºC. In the case of 1200ºC Ar annealing, SOI layer was completely vanished.

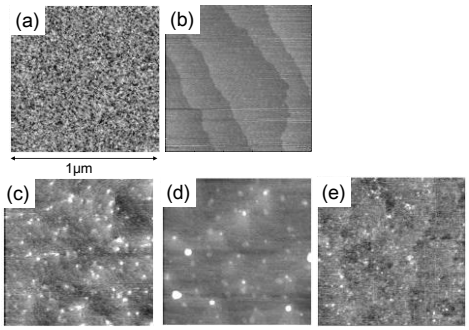

Fig. 4 AFM images of the active region of field-oxide isolated patterns. (a) Initial condition. (b) After Ar annealing at 900 ºC (1 hour) in the case of thermal-SiO_2 field oxide. The atomically flat surface was obtained. (c) and (d) after Ar annealing at (c) 850 ºC (3 hours) and (d) 900 ºC (3 hours) in the case of NSG field oxide. Atomically flat surface was not obtained. (e) The case of non-patterned bare Si wafer surface after Ar annealing at 900 ºC (1 hour) with intentionally-added 20 ppm O_2, showing that surface structure was similar as those of (c) and (d).

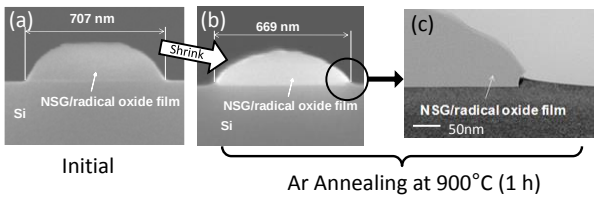

Fig. 5 SEM images of NSG field-oxide film at the edge of active region (a) before and (b) after Ar annealing at 900ºC (1 hour), and (c) shows extended image of edge region in (b) obtained by TEM. NSG film shrank due to the Ar annealing, and a shape anomaly at the edge was observed

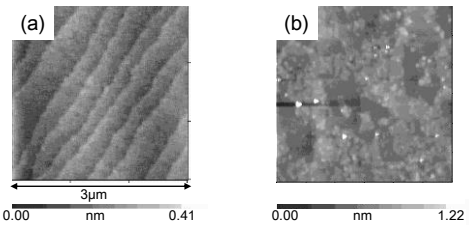

Fig. 6 AFM images of the active region (p-well) of STI pattern after Ar anneal at (a) 850 ºC (5 hours) and (b) 900 ºC (6 hours). Atomically flat Si surface was successfully obtained for Ar annealing at 850 ºC

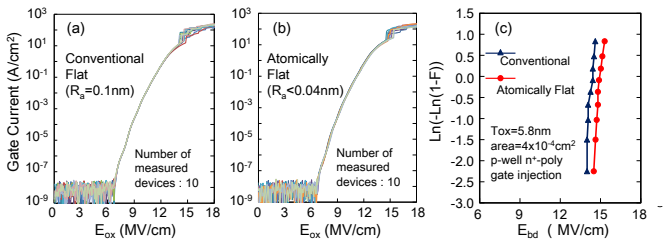

Fig. 7 Gate current as a function of electric field E_{ox} applied in the oxide films of MOS capacitors having STI edge for (a) the reference and (b) atomically flat case. (c) Weibull plot on breakdown E_{ox} intensity (E_{bd}) of these MOS capacitors, demonstrating that E_{bd} of atomically flat case is larger than that of conventional case.